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NEW APPLICATION TRANSMITTAL
UTILITY

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Sir:

Transmitted herewith for filing is a **utility** patent application:

Inventor(s): Steven A. Gronemeyer

Title: SIGNAL DETECTOR EMPLOYING COHERENT INTEGRATION

I. PAPERS ENCLOSED HEREWITH FOR FILING:

55 Page(s) of Specification (including 4 pgs claims)

1 Page(s) Abstract

15 Sheets of Drawings Informal XX Formal

II. ADDITIONAL PAPERS ENCLOSED IN CONNECTION WITH THIS FILING:

☒ Combined Declaration and Power of Attorney (unsigned).

☐ Assignment to and assignment cover sheet.

☐ Verified Statement establishing "Small Entity" under 37 CFR §§ 1.9 and 1.27.

☐ Priority Document No(s): .

☐ Information Disclosure Statement w/PTO 1449 ☐ References

SD-109424.1

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- ☐ 37 CFR § 1.16(e) – **(Surcharge for filing the basic filing fee and/or Declaration on a date later than the filing date of the application)**
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Respectfully submitted,

LYON & LYON LLP

Dated: March 30, 1999

By: _____



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S P E C I F I C A T I O N

SIGNAL DETECTOR EMPLOYING COHERENT INTEGRATION

BACKGROUND

I. Field of the Invention

This invention relates to the field of signal detection using correlation analysis, and more specifically, to correlation analysis in which coherent integration is employed in order to more rapidly achieve a target signal to noise ratio (SNR).

II. Background of the Invention

The Global Positioning System (GPS) is a collection of 24 earth-orbiting satellites. Each of the GPS satellites travels in a precise orbit about 11,000 miles above the earth's surface. A GPS receiver locks onto at least 3 of the satellites, and responsive, thereto, is able to determine its precise location. Each satellite transmits a signal modulated with a unique pseudo-noise (PN) code. Each PN code comprises a sequence of 1023 chips which are repeated every millisecond consistent with a chip rate of 1.023 MHz. Each satellite transmits at the same frequency. For civil applications, the frequency is known as L1 and is 1575.42 MHz. The GPS receiver receives a signal which is a mixture of the transmissions of the satellites that are visible to the receiver. The receiver detects the transmission of a particular satellite by correlating the received signal with shifted versions of the PN code for that satellite. If the level of correlation is sufficiently high so that there is a peak in the level of correlation achieved for a particular shift and PN code, the receiver detects the transmission of the satellite corresponding to

the particular PN code. The receiver then uses the shifted PN code to achieve synchronization with subsequent transmissions from the satellite.

The receiver determines its distance from the satellite by determining the code phase of the transmission from the satellite. The code phase (CP) is the delay, in terms of chips or fractions of chips, that a satellite transmission experiences as it travels the approximately 11,000 mile distance from the satellite to the receiver. The receiver determines the code phase for a particular satellite by correlating shifted versions of the satellite's PN code with the received signal after correction for Doppler shift. The code phase for the satellite is determined to be the shift which maximizes the degree of correlation with the received signal.

The receiver converts the code phase for a satellite to a time delay. It determines the distance to the satellite by multiplying the time delay by the velocity of the transmission from the satellite. The receiver also knows the precise orbits of each of the satellites. Updates to the locations of the satellites are transmitted to the receiver by each of the satellites. This is accomplished by modulating a low frequency (50 Hz) data signal onto the PN code transmission from the satellite. The data signal encodes the positional information for the satellite. The receiver uses this information to define a sphere around the satellite at which the receiver must be located, with the radius of the sphere equal to the distance the receiver has determined from the code phase. The receiver performs this process for at least three satellites. The receiver derives its precise location from the points of intersection between the at least three spheres it has defined.

The Doppler shift (DS) is a frequency shift in the satellite transmission caused by relative movement between the satellite and the receiver along the line-of-sight (LOS). It

can be shown that the frequency shift is equal to $\frac{v_{LOS}}{\lambda}$, where v_{LOS} is the velocity of the relative movement between the satellite and receiver along the LOS, and λ is the wavelength of the transmission. The Doppler shift is positive if the receiver and satellite are moving towards one another along the LOS, and is negative if the receiver and satellite are moving away from one another along the LOS.

The Doppler shift alters the perceived code phase of a satellite transmission from its actual value. Hence, the GPS receiver must correct the satellite transmissions for Doppler shift before it attempts to determine the code phase for the satellite through correlation analysis.

The situation is illustrated in Figure 1, which shows a GPS receiver 200 and three GPS satellites 201a, 201b, and 201c. Each satellite 201a, 201b, 201c is transmitting to the GPS receiver 200. Satellite 201a is moving towards the GPS receiver 200 along the LOS at a velocity v_a^+ ; satellite 201b is moving away from the GPS receiver 200 along the LOS at a velocity v_b^- ; and satellite 201c is moving away from the GPS receiver 200 along the LOS at a velocity v_c^- . Consequently, assuming a carrier wavelength of λ , the

transmission from satellite 201a will experience a positive Doppler shift of $\frac{v_a^+}{\lambda}$; the transmission from satellite 201b will experience a negative Doppler shift of $\frac{v_b^-}{\lambda}$; and the transmission from satellite 201c will experience a negative Doppler shift of $\frac{v_c^-}{\lambda}$.

The GPS receiver functions by sampling the received signal over a defined sampling window and then processing the samples. The duration of the sampling

5 window is chosen to achieve a target signal to noise ration (SNR). The target SNR is chosen to permit the presence and range of the satellites to be accurately detected. If the duration is too short, the signal may be such that there is no correlation value for a particular set of hypotheses which is significantly larger than the correlation values resulting from the other hypotheses tested. The duration of the sampling window must then be increased in order to increase the signal to noise ratio of the received signal, and permit the presence and range of satellites visible to the receiver to be accurately detected.

In addition to the biphasic PN modulation of the GPS carrier, there is also a 50 Hz data modulation. This superimposed data modulation carries information about the satellite orbits. In order to navigate, the system must collect this data so that the locations of the satellites can be calculated as a function of time. This is a necessary piece of information for determining the range to the satellite from the PN code phase. At 50 Hz, the data causes unknown phase flips every 20 milliseconds or data epoch.

GPS receivers typically function by achieving synchronization with certain ones of the satellite, and then maintaining synchronization in a continuous tracking mode of operation. However, in certain applications, such as those involving low power consumption or inherently low C/No, as when operating inside of buildings, an intermittent or code tracking only mode of operation is employed in which a reduced tracking loop bandwidth is used to maintain loop SNR. For example, when C/No falls below 26-28 dB-Hz, data collection and carrier tracking are no longer possible, and GPS receivers change to the code track only mode in which is not possible to receive the 50 Hz data streams to derive bit sync.

In applications such as these, prior art receivers typically attempt to detect a signal of interest or a parameter of the signal of interest by multiplying the segment of samples by a hypothesis about the signal of interest, and then non-coherently integrating the resulting product values over the duration of the sampling window. Non-coherent integration is employed because the phase reversals at the data epochs are unknown, and phase inversions on opposite sides of an inversion point subtract. The result is a decrease in the signal voltage with integration time rather than an increase as desired. In a typical implementation, the magnitude of successive ones of the product values are added together, and phase information represented by the successive values is ignored. The result is a correlation value which is a measure of the degree of correlation between the segment of samples and the hypothesis.

The problem is that noise which may be and typically is reflected in the product values has a magnitude, and when the product values are added together, the magnitude of the noise which is present in each of the values accumulates incrementally in the final sum due to the non-coherent integration procedure. In other words, noise from successive intervals does not have a chance to cancel out the noise from previous intervals. Since the noise magnitudes for successive values add together, the cumulative effect of the noise in the final correlation value can be quite substantial.

Due to the cumulative effects of the noise, the duration of the sampling window has to be substantially increased to achieve a target SNR. The result is that the time required for the GPS receiver to achieve synchronization with satellites visible to it is dramatically increased. In addition, the power consumed by the receiver is also dramatically increased. The problem is particularly acute for applications involving

integrating a GPS receiver with a mobile wireless handset. The consumption of excessive power by such a device drains battery power, and reduces the call-time available from the handset.

Consequently, there is a need for a signal detector which overcomes the disadvantages of the prior art. Similarly, there is a need for a GPS receiver which overcomes the disadvantages of the prior art.

RELATED APPLICATIONS

This application is related to U.S. Patent Application Serial No. 09/145,055, filed September 1, 1998, and entitled "DOPPLER CORRECTED SPREAD SPECTRUM MATCHED FILTER," and to U.S. Patent Application Serial No. __/____, Lyon & Lyon Dkt. No. 241/151, filed on even date herewith, and entitled "SIGNAL DETECTOR EMPLOYING CORRELATION ANALYSIS OF NON-UNIFORM AND DISJOINT SAMPLE SEGMENTS," both of which are owned in common by the assignee hereof, and both of which are hereby fully incorporated by reference herein as though set forth in full.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates an example environment for operation of a GPS receiver.

Figure 2 illustrates an embodiment of a signal detector in accordance with the subject invention.

Figure 3 illustrates an embodiment of a method of operation of a signal detector in accordance with the subject invention.

Figure 4 illustrates a second embodiment of a signal detector in accordance with the subject invention.

Figure 5 illustrates a second embodiment of a method of operation of a signal detector in accordance with the subject invention.

Figure 6 illustrates a third embodiment of a signal detector in accordance with the subject invention.

5 Figure 7 illustrates a third embodiment of a method of operation of a signal detector in accordance with the subject invention.

Figure 8 illustrates an embodiment of a GPS receiver in accordance with the subject invention.

Figure 9 illustrates an embodiment of a matched filter in accordance with the subject invention.

Figure 10 illustrates an embodiment of a method of operation of a GPS receiver in accordance with the subject invention.

Figure 11 illustrates the data structures output by one embodiment of a matched filter in accordance with the subject invention.

Figure 12 illustrates the process of updating data structures in one embodiment of a matched filter in accordance with the subject invention.

Figures 13A-13C illustrates three alternative embodiments of a method of operation of a matched filter in accordance with the subject invention.

SUMMARY OF THE INVENTION

20 In accordance with the purpose of the invention as broadly described herein, there is provided a signal detector which employs correlation analysis to test alternative hypotheses regarding a signal of interest, or a parameter of a signal of interest, in a received signal, and which also employs coherent integration to derive the correlation

values representative of the degree of correlation between each of the hypotheses and the received signal. The received signal comprises the signal of interest perturbed by noise or pseudo-noise. The precise constitution of the received signal is unknown at the receiver. The receiver tests various hypotheses about the presence of a signal of interest, or a parameter of the signal of interest, in the received signal, through correlation analysis. The hypothesis which yields a peak in the correlation values is selected as the correct hypothesis.

The present invention is particularly applicable to low C/N_0 or duty-cycled, low power operation applications of a GPS receiver in which the GPS waveform is not tracked continuously, so that bit synchronization, the location of data epochs, and phase reversals at the data epochs, is not derived from the GPS waveform itself, but rather from another source, such as over a cell phone network, base station or the like, which is capable of providing timing information regarding the GPS system.

In one embodiment, data representative of a hypothesis is multiplied by complex samples of the received signal over a defined duration of time. A complex sample is one which has real and imaginary components, or equivalently, has magnitude and phase components. A complex sum of the samples is determined by coherently adding together the resulting product values over the defined duration such that the phase information which is present in each of the samples, and which is reflected in each of the product values, is maintained. The correlation values which are produced are complex correlation values.

In a second embodiment, a signal of interest is divided up into frames, and may be subject to phase reversals at the boundaries between frames. A segment of samples of the

received signal may cross a frame boundary of the signal of interest. In this second embodiment, a detector detects the phase reversals, and, in response thereto, flips the sign of the samples in the ensuing frame. That allows the coherent integration to cross frame boundaries.

5 In a third embodiment, in which the signal of interest is again divided up into frames, and may be subject to phase reversals at the boundaries between frames, a detector detects the frame boundaries, but does not detect whether a phase reversal has occurred at the boundary. In this embodiment, coherent integration is carried out up to the frame boundary, and the result put aside in a temporary storage location for the hypothesis being tested. Coherent integration is then carried out beginning on the other side of the frame boundary. When this is completed, the value stored in the temporary storage location is retrieved and non-coherently combined with the current value.

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20 In a fourth embodiment, in which the signal of interest is again divided up into frames, and subject to phase reversals at the frame boundaries, a detector detects the frame boundaries, but not necessarily the phase reversals. According to this embodiment, coherent integration is carried out up to the frame boundary, and from that period forward, the coherent integration is continued in parallel under alternate hypotheses about the phase of the signal of interest at the frame boundary. According to one alternate hypothesis, the phase is assumed to remain the same. According to a second alternate hypothesis, the phase is assumed to have flipped at the frame boundary. When the integration is complete, the phase hypothesis which yields the largest value of the integration is assumed to be the correct one.

In one application, the signal detector of the invention is part of a GPS receiver.

In this embodiment, the GPS receiver comprises a radio frequency (RF) receiver, sampling circuitry, timing circuitry, a PN code generator, a matched filter, and a GPS processor. The RF receiver demodulates the received signal to obtain a baseband signal.

5 The sampling circuitry provides, responsive to timing signals produced by the timing circuitry, a segment of samples of the baseband signal taken over a defined sampling window. The matched filter processes the segment of samples in accordance with a plurality of PN code, Doppler shift, and code phase hypotheses.

In one implementation, the signal of interest is a repeating PN code modulated by a lower frequency binary data signal. The period of the data signal defines a frame. If the data value switches state at the frame boundary, the signal of interest is subject to a phase reversal.

In this implementation, the matched filter operates at a time on a segment of samples in which the segment may cross frame boundaries. In one implementation example, the duration of a segment is that of a frame. That way, each segment will cross at most one frame boundary.

In this implementation, the matched filter outputs correlation data derived by correlating various combinations of PN code, Doppler shift and code phase hypotheses with the segment of samples. According to this implementation, the correlation data can be grouped into groupings which correspond to various combinations of specific
20 hypotheses and ranges of hypotheses. In one implementation example, the correlation data comprises a plurality of arrays, wherein each array corresponds to a PN code hypothesis, each row of an array corresponds to a Doppler shift hypothesis, each column

of an array corresponds to a code phase hypothesis, and each entry in the array is a measure of the degree to which the combined PN code, Doppler shift, and code phase hypothesis corresponding to the entry correlates to the samples in the segment.

5 The PN code generator generates the PN code hypotheses which are provided as inputs to the matched filter. In one embodiment, the Doppler shift hypotheses are generated internally within the matched filter. The GPS processor sends out data capture commands to the sampling circuitry and the matched filter directs the sampling circuitry to capture a segment of samples, and directs the matched filter to process the segment of samples.

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20 In one embodiment, the samples are complex samples, and each segment of samples is divided into incremental portions or subsegments, and processed one subsegment at a time. In one implementation, the duration of a subsegment is selected such that an integral number of subsegments fits within a frame. In one implementation example, the correlation data resulting from processing a given subsegment of complex samples comprises a plurality of complex arrays, wherein each array in the plurality corresponds to a particular PN code hypothesis, and each row of an array corresponds to a particular Doppler shift hypothesis. Cumulative correlation arrays are maintained and initialized with the correlation arrays for the first subsegment. Then, the correlation arrays for the second subsegment are combined through complex addition with the cumulative correlation arrays one array element at a time. The process continues for each of the subsegments in the segment of samples.

In one implementation, a detection circuit detects frame boundaries and phase reversals imposed by the data signal at the frame boundaries. If the detection circuit

indicates a phase reversal at a frame boundary, the phase of the ensuing samples is reversed. In one implementation example, this is accomplished by flipping the sign of the complex phasor generated by a Doppler generator circuit to correct for Doppler shift. A complex mixer multiplies the complex samples of the received signal by the complex phasor. By flipping the sign of the complex phasor, the sign of the ensuing samples is effectively reversed. Coherent integration may thus proceed across the frame boundary.

In a second implementation, a detector circuit detects the frame boundary, but not necessarily the phase reversal at the frame boundary. In this implementation, coherent integration is carried out up to the frame boundary, and the result stored in temporary storage. The cumulative data is then reset, and coherent integration resumed on the other side of the frame boundary. When this has been completed, the results in temporary storage represent coherent integration over a first portion of the segment, and the current cumulative values represent coherent integration over a second remaining portion of the segment.

According to the second implementation, these results are non-coherently combined. In one implementation example, a procedure is employed in which the magnitude of each complex correlation value is determined by taking the square root of the sum of the squares of the real and imaginary part of each value. This procedure is employed for each correlation value in temporary storage representative of the first portion of the segment, and each correlation value representative of the second portion of the segment. The magnitude values are then combined by simply adding corresponding values together for the first and second portions.

In a third implementation, a detection circuit again detects frame boundaries, but not necessarily the phase reversals at the frame boundaries. Again, coherent integration is carried out up to a frame boundary. Then, the results are replicated for a plurality of alternative hypotheses about the phase reversal. In one implementation example, the results are replicated once, such that a total of two integrations are carried out in parallel, each corresponding to an alternative hypothesis regarding phase reversal. According to this implementation example, one hypothesis is that phase is unchanged across the frame boundary, and the other is that the phase has flipped across the frame boundary. Coherent integration then proceeds across the frame boundary, with multiple integrations being conducted in parallel consistent with the alternative phase hypotheses. At the conclusion of this process, a determination is made of which phase hypothesis yields the greatest correlation values. The phase hypothesis which does so is then selected as the correct hypothesis, and the correlation values corresponding to this phase hypothesis are selected as the correct ones for the other hypotheses involved.

By coherently integrating the product data for a given hypothesis, the subject invention is able to achieve a target SNR in the resulting correlation data in a shorter amount of time. The reason is that successive samples of noise perturbing successive signal samples tends to cancel itself out when the phase information thereof is taken account of through coherent integration. The result is that a signal detector or GPS receiver in accordance with the subject invention is faster and consumes less power than prior art detectors and receivers.

Related methods of operation and computer readable media are also provided.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

5 A block diagram of one embodiment of a signal detector in accordance with the subject invention is illustrated in Figure 2. As illustrated, the signal detector comprises a receiver 2000 configured to receive a signal, and provides samples thereof. The signal may comprise a signal of interest perturbed by noise. Alternatively, in accordance with a spread spectrum environment, the signal may comprise the combination of multiple signals of interest each encoded or modulated using one of a plurality of pseudo-noise (PN) codes. In this case, other signals appear as noise to a particular signal of interest. The samples of the signal each have real and imaginary components, or equivalently, magnitude and phase components. In one implementation, each sample of the signal has in-phase (I) and quadrature (Q) components which can be represented as a complex number of the following form: $I+jQ$.

10 A hypothesis generator 2001 generates a plurality of hypotheses about the signal of interest. A correlator 2030 is provided which comprises a multiplier 2002 and a coherent integrator 2003. The multiplier 2003 receives the plurality of hypotheses from hypothesis generator 2001, and samples of the signal received by receiver 2000, and responsive thereto, generates product data representative of the product of the samples of the received signal and data representative of each of the plurality of generated hypotheses.

20 The product data is provided to coherent integrator 2003, which coherently integrates the product data for a given hypothesis over a defined duration, that is to say, the coherent integrator 2003 takes account of the phase information for the samples of received 2000 which are reflected in the product data for a given hypothesis. Each of the

product values have real and imaginary components, or equivalently, magnitude and phase components, and coherent integration is achieved by separately integrating the real and imaginary, or equivalently the magnitude and phase components, of the product values. The result is a correlation value, having real and imaginary components, or
5 equivalently, magnitude and phase components, for the given hypothesis which measures the degree of correlation between the given hypothesis and the received signal.

The foregoing procedure is repeated for each of the hypotheses of interest generated by hypothesis generator 2001. The result is that a plurality of correlation values are output by the coherent integrator 2003, each corresponding to a given hypothesis, and each having real and imaginary, or equivalently, magnitude and phase components.

These correlation values are then analyzed, and, responsive thereto, one of the tested hypotheses is selected as the correct one. In one implementation, this is accomplished through peak detection, according to which a correlation value is selected which has a significantly larger magnitude than that of the other correlation values. The hypothesis corresponding to this correlation value is then selected as the correct hypothesis.

A flowchart of a method of operation of a signal detector in accordance with the foregoing embodiment of the subject invention is illustrated in Figure 3. As illustrated,
20 the process begins at step 10, in which a segment of samples of a signal is received. Typically, the signal comprises a signal of interest perturbed by noise or pseudo-noise.

Then, in step 11, a plurality of hypotheses are generated for testing. In step 12, one of the hypotheses from step 11 is selected, and in step 13, the product is formed

between the samples of the signal and data representative of the hypothesis selected in step 12.

In step 14, the product data resulting from step 13 is coherently integrated over a defined duration, and in step 15, a correlation value is derived from the coherent integration performed in step 14, and saved for the hypothesis. In step 16, a determination is made whether there are any additional hypotheses of the plurality generated in step 11 that remain to be tested. If so, a jump is made to step 12, and the process beginning at this point repeats itself for one of the remaining hypotheses. If not, the process terminates.

A second embodiment of a signal detector in accordance with the subject invention is illustrated in Figure 4, in which, compared to Figure 2, like elements are referenced with like identifying numerals.

In this embodiment, the receiver 2000 receives a signal, which typically is a signal of interest perturbed by noise or pseudo-noise. The signal of interest is subject to phase reversals which occur at defined frame boundaries. In one implementation, these phase reversals occur due to a low frequency data signal which is modulated onto a higher frequency signal comprising a repeating PN code modulated onto a carrier signal. The receiver 2000 samples the signal and provides the samples to multiplier 2002 which, together with coherent integrator 2002, comprises correlator 2030.

As before, hypothesis generator 2001 generates a plurality of hypotheses to be tested, and provides the same to multiplier 2002. Multiplier 2002, responsive to the hypotheses generated by hypothesis generator 2001 and the samples from receiver 2000,

forms the product between the samples and each of the hypotheses and provides the resulting product data to coherent integrator 2003.

Phase reversal detector 2005 is also provided. In one implementation, it is external to the signal detector. In another, it is internal to the signal detector. In the implementation in which the phase reversal detector is internal to the signal detector, it receives timing and other information from receiver 2000 regarding the received signal, and, responsive thereto, detects instances where the signal of interest undergoes a phase reversal at a frame boundary. This information is provided to coherent integrator 2003, which uses this information to coherently integrate the product values provided by multiplier 2002.

In applications in which the phase reversal detector is external to the signal detector, the phase reversal detector detects phase reversals from a source of information other than the waveform from which the samples are derived. In one example, the phase reversal detector is part of a call or PCS phone, and detects phase reversals based on timing information provided to it from the base station servicing the phone in the cellular network.

Coherent integrator 2003 receives the product values from multiplier 2002, and the phase reversal information from phase reversal detector 2005, and, responsive thereto, coherently integrates the product values for a given hypothesis while adjusting for phase reversals that may occur at frame boundaries. The phase reversals must be accounted for to ensure that successive product values subject to the phase reversal add constructively, rather than destructively, to the partial correlation value accumulated from the product values not subject to the phase reversal. In one implementation, this is accomplished by

flipping the sign of the samples input to multiplier 2002 upon the detection of a phase reversal by phase reversal detector 2005.

Coherent integrator 2003 then provides correlation values for each of the hypotheses generated by hypothesis generator 2001, in which each of the correlation values are determined by taking account of the phase reversals detected by phase reversal detector 2005.

A method of operation of a signal detector in accordance with the foregoing embodiment is illustrated in Figure 5. As illustrated, the process begins at step 2013, in which a segment of samples of a signal is received. Typically, the signal comprises a signal of interest perturbed by noise or pseudo-noise. In addition, the signal of interest is subject to phase reversals at defined frame boundaries.

In step 2007, a plurality of hypotheses are generated regarding the signal of interest, or a parameter of the signal of interest. In step 2008, one of the hypotheses from step 2007 is selected for testing. The received samples are then divided up into incremental portions or subsegments.

In step 2009, the product between the next incremental portion of the samples and data representative of the hypothesis selected in step 2008 is formed. In step 1010, coherent integration is performed over the product values resulting from step 2009. In step 2011, a determination is made whether the ensuing incremental portion of samples is at a frame boundary, and whether there is a phase reversal at the frame boundary. If both conditions are present, step 2012 is performed. If not, the process proceeds directly to step 2014, bypassing step 2012.

In step 2012, an adjustment is made to take account of the phase reversal to ensure that subsequent product values add constructively, rather than destructively, to the accumulated integration value. In one embodiment, this step comprises flipping the sign of the ensuing samples until the next phase reversal is detected. The process then
5 proceeds to step 2014.

In step 2014, a determination is made whether the integration is complete for the selected hypothesis, that is, whether there are any remaining incremental portions of the received samples that remain to be processed for the selected hypothesis. If the integration is not complete, the process jumps to step 2009, and the process repeats itself beginning at this point. If the integration is complete for the hypothesis, step 2015 is performed. In step 2015, a correlation value for the hypothesis is derived from the integration, and stored. Step 2016 is then performed. In step 2016, a determination is made whether there are more hypotheses to be tested. If so, a jump is made to step 2008, and the process beginning at this point is repeated for the next hypothesis to be tested. If not, the process ends.

A third embodiment of a signal detector in accordance with the subject invention is illustrated in Figure 6 in which, compared to Figures 2 and 4, like elements are referenced with like identifying numerals. In this embodiment, receiver 2000 receives a signal which, as in the Figure 4 embodiment, comprises a signal of interest perturbed by noise or pseudo-noise, and is subject to phase reversals at defined frame boundaries. The
20 receiver 2000 provides multiplier 2002 with samples of the signal.

Hypothesis generator 2001 generates a plurality of hypotheses for testing. Correlator 2030 comprises multiplier 2002, coherent integrator 2003, and noncoherent

integrator 2022. Multiplier 2002, responsive to the hypotheses from hypothesis generator 2001 and the samples from receiver 2000, produces data representative of the product of the samples and data representative of each of the hypotheses to be tested.

5 A frame detector 2020 is also provided, either internally, as part of the signal detector, or externally, such as from a cellular or PCS phone. In an implementation in which the frame detector is internal to the signal detector, the frame detector receives timing information from the receiver 2000, and, responsive thereto, detects the boundaries between frames, and provides a signal to coherent integrator 2003 containing this information. In an implementation in which the frame detector is external to the signal detector, the frame detector receives timing information from a source other than the waveform from which the samples are derived. In one implementation example, this timing information is obtained from a cellular, wireless or PCS network.

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20 Coherent integrator 2003 receives the product values from multiplier 2002, and the information about frame boundaries from frame detector 2020, and, responsive thereto, coherently integrates the product values for a given hypothesis up to a frame boundary. When a frame boundary is detected, the partial integration value is stored in a temporary location for the hypothesis, and then the partial integration value reset for the hypothesis. Coherent integration is then resumed for the samples on the other side of the frame boundary. If another frame boundary is detected, the foregoing is repeated. This procedure is repeated for each of the hypotheses to be tested.

At this point, there are a plurality of integration values stored for each hypothesis, with each of the integration values representing the coherent integration of product values between, but not crossing, frame boundaries. This information is then provided to

noncoherent integrator 2022. Noncoherent integrator 2022 receives this information, and, responsive thereto, noncoherently combines the coherent integration values for a given hypothesis. In one implementation, each of the integration values has a real and an imaginary component, and the magnitude of the integration value is obtained by taking the square root of the sum of the squares of the real and imaginary components. The magnitude values for a given hypothesis are then added together to arrive at a correlation value for the hypothesis. The foregoing procedure is then repeated for each of the hypotheses.

A method of operation of a signal detector in accordance with this third embodiment is illustrated in Figure 7. In step 100, a segment of samples of the signal is received. In step 101, a plurality of hypotheses regarding the signal of interest are generated. In step 102, one of the hypotheses is selected. In step 103, the product between the samples and data representative of the hypothesis is formed. The resulting product values are then divided up into a plurality of incremental portions or subsegments.

In step 104, the next incremental portion of product values for the selected hypothesis are coherently integrated. In step 105, a determination is made whether a frame boundary has been detected. If so, step 106 is performed. If not, step 106 is bypassed, and step 109 performed directly.

In step 106, the current integration value for the hypothesis is noncoherently combined with any previous integration values obtained for previous frames. In one implementation, the magnitude of the current integration value is obtained by taking the square root of the sum of the squares of the real and imaginary components thereof, or

equivalently, the sum of the squares of the real and imaginary components. This value is then added to the magnitudes which have been derived for the hypothesis for previous frames.

5 In step 109, a determination is made whether the integration has been completed for the current hypothesis. If not, a jump is made to step 104, and the process repeated at this point for the next incremental portion of product values. If so, the process ends.

At the conclusion of the process, a plurality of correlation values are available, with a correlation value corresponding to each of the hypotheses tested.

It is contemplated that the foregoing signal detector can be beneficially employed in a variety of applications, such as in a GPS receiver. The present invention is particularly applicable to low C/N_0 or duty-cycled, low power operation applications of a GPS receiver in which the GPS waveform is not tracked continuously, but only intermittently. In applications such as this, information about bit synchronization, the location of data epochs, and phase reversals at the data epochs is not directly available from the GPS waveform itself, but must be derived from another source, such as a cell or PCS phone network or base station, or a local clock periodically synchronized with the atomic clocks maintained on the GPS satellites.

One embodiment of a GPS receiver in accordance with the subject invention is illustrated in Figure 8. As shown, the receiver comprises a radio frequency (RF) receiver
20 300, sampling circuitry 308, timing circuitry 307, a PN code generator 312, a matched filter 310, and a GPS processor 303. In one embodiment, a signal is received by GPS receiver 300 which comprises a plurality of signals, each from a satellite visible to the receiver. Each satellite signal comprises a repeating PN code unique to the satellite.

Each period of the PN code comprises 1023 chips which repeats every 1 mS, for a nominal chip rate of 1.023 MHz. Each satellite signal is modulated with a 50 Hz data signal. The period of the data signal, 20 mS, defines a frame. One purpose of the data signal is to convey locational information about the satellite to the receiver.

5 The data signal is capable of changing state every 20 mS period, that is, at a frame boundary. If the data signal changes state, the underlying signal undergoes a phase reversal. If the data signal remains the same, the phase of the underlying signal remains the same.

 The RF receiver section 300 demodulates the received signal to obtain a baseband signal which is provided to the sampling circuitry 308 over signal line 302. The sampling circuitry 308 provides, responsive to timing signals produced by the timing circuitry 307, a segment of samples of the baseband signal taken over a defined sampling window. The segment of samples is provided to the matched filter 310 over signal line 309. The matched filter 310 processes the segment of samples in accordance with a plurality of PN code, Doppler shift, and code phase hypotheses.

 In one implementation, as illustrated in Figure 11, for each segment of samples, the matched filter outputs a plurality of correlation arrays 600, 601, 602 of data derived from the segment of samples. According to this implementation, each array 600, 601, 602 corresponds to a PN code hypothesis, PN1, PN2, . . . PNr, each row of an array 600, 601, 602 corresponds to a Doppler shift hypothesis, DS1, DS2, . . . DS_m, each column of an array 600, 601, 602 corresponds to a code phase hypothesis, CP1, CP2, . . . CP_n, and each entry in an array 600, 601, 602 is a measure of the degree to which the combined PN code, Doppler shift, and code phase hypothesis corresponding to the entry correlates to

the samples. Thus, in Figure 11, numeral 500 identifies a correlation array corresponding to PN code hypothesis PN1; numeral 501 identifies a correlation array corresponding to PN code hypothesis PN2; and numeral 502 identifies a correlation array corresponding to PN code hypothesis PNr.

5 The PN code generator 312 generates the PN code hypotheses which are provided as inputs to the matched filter 310 over signal line 315. In one embodiment, the Doppler shift hypotheses are generated internally within the matched filter. The GPS processor 303 issues data capture commands on signal line 314 to the sampling circuitry 308 and the matched filter 310. Each data capture command directs the sampling circuitry 308 to capture a segment of samples, and also directs the matched filter 310 to process the segment of samples. The timing circuitry 307 generates, responsive to first timing signals provided by receiver 300, second timing signals which are provided as inputs to the sampling circuitry 308 and the matched filter 310. In one implementation, the first timing signals generated by the RF receiver 300 are generated by a local oscillator within the RF receiver, and define a local time base which is related to the time base maintained by the GPS satellites.

10 In one embodiment, the correlation arrays for a segment are grouped by PN code hypothesis, and by Doppler shift hypothesis for a given PN code hypothesis. The result is that each grouping corresponds to a particular combination of PN code hypothesis and
20 Doppler shift hypothesis. In one implementation example, the correlation arrays corresponding to a satellite are used to detect the presence and range of the satellite. Typically, this occurs when the correlation data for a particular set of hypotheses is significantly greater than the correlation data for alternative hypotheses.

Figure 9 illustrates one embodiment of matched filter 310 in Figure 8. Compared to Figure 8, like elements in Figure 9 are referenced with like identifying numerals. As illustrated, this embodiment of the matched filter comprises random access memory (RAM) 400 which is configured to receive a segment of samples from sampling circuitry 308 over signal line 309. In one implementation example, a segment is 20 mS in duration, the same as the frame duration, and the RAM 400 is configured to receive one 20 mS segment of samples at a time. According to this implementation example, each 20 mS segment of samples comprises 40920 samples, obtained by sampling the baseband signal at a nominal sampling rate of 20.46 MHz, and then performing decimation filtering. Note that, in this implementation example, although a segment has the same duration as a frame, in general, frame boundaries will not occur synonymously with segment boundaries, and in fact, will typically occur between segment boundaries.

Each sample is a complex sample having an in-phase (I) component and a quadrature (Q) component which can be represented in complex form as $I+jQ$. In one implementation example, each component can take on the values -1 , 0 , and $+1$, and thus can be represented with 2 bits. In this implementation example, each sample can be represented with 4 bits, and a 20 mS frame of samples requires $40,920 \times 4 \text{ bits} = 163\text{K bits}$ of RAM 400 for the storage thereof.

In one implementation, the matched filter of Figure 9 is configured to divide up the segment of samples in to 1 mS incremental portions or subsegments, the same duration as the PN code period, and to process a 1 mS subsegment at a time. In this implementation example, each 1 mS subsegment of samples comprises 2046 samples, each having I and Q components, each such component represented by 2 bits.

The matched filter further comprises complex mixer 403, and incremental Doppler generator 401. In one implementation, the RAM 400 is configured to provide to complex mixer 403 over signal line 404 a 1 mS subsegment of samples from the segment stored therein at a time.

Incremental Doppler generator 401 generates a plurality of Doppler shift hypotheses which are provided to complex mixer 403 over signal line 405 one hypothesis at a time. In one implementation example, the incremental Doppler generator 401 generates Doppler shift hypotheses in the range of $\pm 62,000$ Hz, to allow for inaccuracy in the local time base that is not corrected by the input sampling process.

Complex mixer 403 receives a subsegment of samples from RAM 400 over signal line 404, and a Doppler shift hypothesis from incremental Doppler generator 401, and, responsive thereto, multiplies the samples by a complex phasor of the form $e^{-jw_d t}$, where w_d represents the Doppler shift hypothesis provided by incremental Doppler generator 401. A Doppler-corrected subsegment of samples results which are stored in sample register 406. Additional detail about this procedure is available in U.S. Patent Application Serial No. 09/145,055, filed September 1, 1998, entitled "DOPPLER CORRECTED SPREAD SPECTRUM MATCHED FILTER," previously incorporated by reference herein as though set forth in full.

In one implementation example, each corrected subsegment of samples continues to comprise 2046 complex samples, each having I and Q components, which can be represented in combination as $I+jQ$, and each of which can take on any one of the discrete values $-2, -1, 0, +1$, and $+2$. In this implementation example, each component

requires 3 bits for the representation thereof, and thus the 2046 samples in a corrected subsegment requires $2046 \times 6 \text{ bits} = 12,276 \text{ bits}$ in register 406 for the storage thereof.

PN code register 415 is provided to store the current PN code hypothesis provided by PN code generator 312 over signal line 315. In one implementation, each PN code hypothesis represents one period of a PN code. In one implementation example, the PN code period is 1 mS, and each PN code hypothesis represents 1023 chips which repeats every 1 mS, representing a chip rate of 1.023 MHz. In this implementation example, the PN code register is configured to store 1023 chips at a time.

As indicated by signal line 414, the PN code register is capable of being circularly shifted by an amount which corresponds to a code phase delay hypothesis. In the implementation example which has been discussed, in which the period of a PN code is 1023 chips, the value of the code phase delay can range from 0 to 2045 half chip increments. The PN code register is configured in this implementation example to be circularly shifted by any number or fraction of chips which correspond to a code phase delay hypothesis under consideration.

Sum of products circuitry 407 is also provided. This circuitry is configured to form the coherent integration of the product between the subframe of corrected samples stored in sample register 406 and the PN code hypothesis stored in the PN code register 414.

In the implementation example discussed earlier in which the subsegment of samples stored in sample register 406 comprises 2046 samples, each having I and Q components, and the PN code hypothesis stored in PN code register 415 comprises 1023 chips, a correspondence is present between two of the samples in the sample register 406,

and one of the chips in PN code register 415. The I and the Q components of each of the two samples is multiplied by the corresponding PN chip. Then, the sum of the I component products is determined, and the sum of the Q component products is separately determined. The sum of the I component products is output on signal line 408, and the sum of the Q component products is output on signal line 409.

In equation form, the function of the sum of products circuitry 407 in this implementation example can be represented as follows:

$$(1) \quad SI = \sum_{i=1}^{1023} CHIP_i \times (I_i^1 + I_i^2)$$

$$(2) \quad SQ = \sum_{i=1}^{1023} CHIP_i \times (Q_i^1 + Q_i^2)$$

where $CHIP_i$ is the i th chip in the PN code hypothesis, I_i^1 is the I component of the first of the two samples corresponding to $CHIP_i$, I_i^2 is the I component of the second of the two samples corresponding to $CHIP_i$, Q_i^1 is the Q component of the first of the two samples corresponding to $CHIP_i$, and Q_i^2 is the Q component of the second of the two samples corresponding to $CHIP_i$.

The matched filter is capable of two modes of operation controlled by the state of coherent switch 433. The state of coherent switch 433 can be set to either “0” or “1” by GPS processor 303. In a first mode of operation, defined when the state of switch 413 is set to “1”, the matched filter is configured to coherently integrate the SI and SQ values which have been computed with corresponding SI and SQ values determined for previous subsegments. In a second mode of operation, defined when the state of switch 413 is set to “0”, the matched filter is configured to non-coherently integrate the SI and SQ values

which have been computed with corresponding SI and SQ values for previous subsegments.

The state of switch 433 controls the state of switches 432a and 432b. When switch 413 is set to “1”, switches 432a and 432b are configured to pass directly to complex adder 411 the SI and SQ values from signal lines 408 and 409, respectively. When switch 413 is set to “0”, switches 432a is configured to pass the output of sqrt. of sum of squares circuit 410 to complex adder 411, and switch 432b is configured to provide a null value to complex adder 411.

Complex adder 411 is configured to perform a complex addition of the two complex values provided at its two inputs, and to store the result in complex RAM 413. One of the inputs to complex adder 411 is provided from complex RAM 413 over signal line 412. The other input is provided from switches 432a and 432b. The sqrt. of sum of squares circuit 410 is configured to receive the SI and SQ values on signal lines 408 and 409 respectively, and to compute the square root of the sum of the squares of these two values. In equation form, the circuit computes the value:

$$(3) \quad SS = \sqrt{(SI)^2 + (SQ)^2} .$$

Sqrt. of sum of squares circuit 431 is configured to receive a complex number from complex RAM 413 and compute the magnitude thereof, that is, the square root of the sum of the squares of the real and imaginary components thereof, or equivalently, the sum of the squares of the real and imaginary components. The result can then be stored back in complex RAM 413 through bus 313.

Peak detector 430 is configured to receive a plurality of correlation values from RAM 413, and, responsive thereto, select a maximum thereof. Once selected, the

maximum value is provided to bus 313, whence it can be provided to GPS processor 303, or to complex RAM 413.

Timing circuitry 307 from Figure 8 provides a clock to timing circuit 435 over signal line 317. Responsive thereto, timing circuit 435 generates a timing pulse for every subsegment. Counter 436 receives the timing pulses from timing circuit 435, and responsive thereto, counts the number of subsegments which have been processed by the matched filter of Figure 9. Register 438 stores the subsegment number at which the next frame boundary will occur. It is configured to be loaded with this number by GPS processor 303 over bus 313. In one implementation, in which a segment duration is 20 mS, and the subsegment duration is 1 mS, a segment boundary will occur every 20 subsegments.

Bit circuitry 439 is configured to store the value of the data signal modulated onto the signal of interest beyond the next frame boundary. It is configured to be loaded with this value by GPS processor 303 over bus 313. Bit circuitry 439 is also configured, responsive to the detection of a frame boundary by compare circuit 437, and the state of the next data bit, to determine whether there will be a phase reversal in the signal of interest at the segment boundary. If the data signal does not change state at the frame boundary, then there will not a phase reversal at the frame boundary. Conversely, if the data signal changes state at the frame boundary, there will be a phase reversal at the frame boundary.

If there is a frame reversal at the frame boundary, the flip signal output from the bit circuitry 439 is asserted. This flip signal is also provided as an input to incremental Doppler generator 401. Responsive to the assertion of this signal, incremental Doppler

generator 401 flips the sign of the complex phasor that is multiplied by the current subsegment of samples by complex mixer 403. Thus, if the sign of the phasor is positive, and the flip signal is then asserted, the sign of the complex phasor will become negative. In equation form, the complex phasor will go from $e^{j\omega_d t}$ to $-e^{j\omega_d t}$. Conversely, if the sign of the phasor is negative, and the flip signal is then asserted, the complex phasor will go from $-e^{j\omega_d t}$ to $e^{j\omega_d t}$. When the modified phasor is multiplied by the incoming samples by complex mixer 403, a phase reversal of the samples is implemented to counteract the phase reversal caused by the change of state of the data signal at the frame boundary.

The data epoch timing and data bit values stored respectively in DE register 438 and Bit circuitry 439 is typically derived from a source other than the GPS waveform from which the samples stored in RAM 400 are derived.

In one embodiment, this information is derived from an accurate clock maintained in the GPS receiver and periodically synchronized with the atomic clocks maintained on the GPS satellites to preserve data epoch timing and data values.

In another embodiment, the GPS receiver would be normally operated in a continuous mode of operation, and then switched to an intermittent mode of operation when low power operation is desired or the C/No value of the received signal is low, such as the case in which the receiver enters a building. A local clock would be synchronized with the atomic clocks maintained at the GPS satellites to provide accurate data epoch timing and data values when the GPS receiver is operating in the continuous tracking mode of operation. The local clock would be capable of providing accurate information

about data epoch timing and data values during the time the receiver is operated in an intermittent mode of operation.

In another embodiment, this information is derived from another source external to the GPS receiver, such as a cellular or PCS phone network or base station. Cellular or
5 PCS networks commonly track the GPS satellites, and are capable of providing this information to a GPS receiver.

In yet another embodiment, the GPS receiver would be periodically operated in a continuous tracking mode of operation to collect ephemeris and almanac data. Ephemeris collection takes 18 seconds and must be done about once an hour. Almanac collection take 6 seconds each and must be collected weekly for each of the 24 satellites. The almanac data is normally constant for a week time and ephemeris data is normally constant over a period of one hour. Consequently, once this information is collected, it can be used to predict data phase changes as a function of time.

There is one aspect that must be considered in this method. Although the ephemeris data normally changes at the top of each hour and the almanac data changes at a known time of the week, the GPS system allows for arbitrary times of changes when necessary. These events normally occur when the GPS control segment uploads new data to the satellites. These uploads occur when the satellites pass over the uplink ground stations, which is typically not at the normal changeover times. Therefore, unexpected
20 changes in the data needs to be accounted for.

Registers 441 and 442 are used to store, respectively, the start address of the samples in the segment of samples stored in RAM 400 that integration is to start at, and the number of mS that the integration is to proceed over. These two registers are

loadable by GPS processor 303 over bus 313. Together, they are used to define an arbitrary portion of the current segment over which integration is to proceed.

In a first mode of operation, switch 433 is set to "1", indicating that coherent integration is to be carried out. A segment of complex samples is stored in RAM 400.

5 One subsegment at a time, the samples are multiplied by a complex phasor to correct for Doppler shift and stored in sample register 406. The samples are then multiplied by the PN code stored in register 415, and the SI and SQ sum of products values computed by circuitry 407. The SI and SQ values are then provided over signal lines 408 and 409 respectively, and added by complex adder 411 to any corresponding values previously stored in complex RAM 413 for previous subsegments of the segment stored in RAM 400.

10 If the subsegment under consideration and stored in sample register 406 is the first subsegment for the segment of interest, the foregoing values are stored in an array entry in RAM 413 corresponding to the combination of the PN code, Doppler shift, and code phase hypotheses under consideration. The arrays are of the same format as those depicted in Figure 11 and will eventually become the correlation arrays for the current segment of samples in RAM 400.

15 If the subsegment under consideration and stored in sample register 406 is not the first subsegment analyzed for the segment of interest, there may already be a value derived from a previous subsegment stored in RAM 413 in the entry corresponding to the combination of the PN code, Doppler shift, and code phase hypotheses under consideration. In this case, the SI and SQ values determined above are added by adder 411 to the previously stored values for the entry which are provided to the adder 411 over

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signal line 412. The result is then stored in lieu of the previously stored values in the array entry corresponding to the combined PN code, Doppler shift, and code phase hypotheses.

5 This process is illustrated in Figure 12. An array 600 represents cumulative values which are stored in memory 413 for previous subsegments of the segment under consideration. Numeral 603 identifies SI and SQ values derived from the current subsegment for a particular PN code, Doppler shift, and code phase hypothesis. The figure illustrates the procedure for updating the cumulative SI and SQ values for entry 602 in array 600 with the corresponding values identified by numeral 603. These cumulative values are retrieved, as indicated by identifying numeral 604, and then added to the corresponding values identified by numeral 603. This addition step is identified by numeral 608. The resulting values, identified by numeral 605, are then restored in lieu of the original values stored in entry 602. This procedure is identified by numeral 609 in Figure 12.

6045 The next code phase hypothesis is then selected, and the PN code register 407 circularly shifted in accordance with the selected code phase hypothesis. The foregoing process is then repeated for the next code phase hypothesis. This process continues for each of the code phase hypotheses which are desired to be tested for the current PN code and Doppler shift hypotheses. In one implementation, 2046 code phases are tested for each 1 mS subsegment, corresponding to the repetition period of the PN codes. In this implementation, the code phase hypotheses which are tested range from 0 to 2045 half-chip increments, and the next code phase hypothesis is selected simply by circularly shifting the PN code register 415 by one-half chip.

The foregoing process is repeated for each of the PN code and Doppler shift hypotheses to be tested. In this manner, the arrays of correlation values stored in RAM 413 are incrementally updated with the values derived for the current subsegment. When all the desired hypotheses have been tested for the current subsegment, the foregoing process is repeated for the next subsegment stored in RAM 400. If a subsegment falls on a frame boundary, and there is a phase flip at the boundary, the flip signal 440 is asserted, causing a change in sign of the complex phasor which will be multiplied by ensuing subsegments of samples. The result is that the phase reversals are accounted for such that the SI and SQ values derived from these subsequent subsegments will add constructively, rather than destructively, to the values accumulating in the correlation arrays stored in RAM 413.

The foregoing process is repeated for each of the subsegments within the portion of the current segment which is defined by the values in registers 441 and 442. When this process has been completed, correlation arrays of the form shown in Figure 11 are present in RAM 413. These correlation arrays are provided to the GPS processor 303 over signal line 313. GPS processor 303 uses these correlation arrays to detect the presence and range of satellites in the manner described previously.

In the second mode of operation, defined to be when the switch 433 is set to "0", the SI and SQ values for the current subsegment are combined noncoherently with corresponding values for previous subsegments in the current segment. Circuitry 410 forms the SS value from the current SI and SQ values. This SS value is then passed through switch 432a to complex adder 411, whereupon it becomes the real part of the first input to the complex adder 411. The imaginary part of this first input is the null

value 434 which is passed through switch 432b. This value is then added to a corresponding value stored in cumulative correlation arrays maintained in RAM 413 in a procedure similar to that described earlier in relation to Figure 12, except that only real values are maintained in the arrays rather than complex values.

5 Third and fourth modes of operation are also possible for the case in which bit circuitry 439 is not provided, and a phase reversal at a frame boundary cannot be detected, although the frame boundary itself can. In one implementation, the detection of the frame boundary is performed by comparator 437, which asserts an output signal when a frame boundary is encountered. In one implementation example, a frame boundary is referred to as a data epoch.

In the third mode of operation, the object is to perform a first coherent integration for the portion of the segment up to the frame boundary, and to perform a second coherent integration for the portion of the segment beyond the frame boundary, and then to noncoherently combine the two integrations. In one implementation, in which a segment has the same duration as a frame, there will be at most one frame boundary encountered as integration proceeds across the segment. In this implementation two sets of arrays of the form shown in Figure 11 are maintained for the current segment. One set of arrays is complex, and is used to accumulate the coherent integration values in the manner described earlier in relation to the first mode of operation. The second set of
20 arrays is real, and is used to noncoherently combine the coherent integrations performed on either side of the frame boundary.

When a frame boundary is encountered, the values in each of the entries in these arrays is put into noncoherent form by circuitry 431, that is, by computing the square root

of the sum of the squares of the real and imaginary values stored in each entry. These values are then stored in the corresponding entries in the second set of arrays. The first sets of arrays are all then reset to zero. Coherent integration is then resumed, and the results thereof accumulated in the first set of arrays. When this has been completed, the values of the first set of arrays are put into noncoherent form in the manner described above. These values are then added to the corresponding values stored in the second set of arrays. The second set of arrays thus becomes the correlation values for the segment.

In the fourth mode of operation, the object is to perform coherent integration up to a frame boundary, and to continue coherent integration beyond that point under two alternative hypotheses, one assuming that there has been no phase reversal at the frame boundary, and the other assuming there has been a phase reversal at the frame boundary.

In the one implementation, in which the segment duration is the same as the frame duration, there will be at most one frame boundary within a segment. In this implementation, two sets of arrays of the form shown in Figure 11 are maintained in RAM 413 for the current segment. Both are complex. The first set of arrays is used to accumulate the results of coherently integrating up to the frame boundary in the manner described. When the frame boundary is detected, the accumulated results are copied into the second set of arrays. Coherent integration is then resumed for the remaining portion of the segment beyond the frame boundary. The first set of arrays is used to accumulate results under the hypothesis that there has been no phase reversal at the frame boundary. The second set of arrays is used to accumulate results under the hypothesis that there has been no phase reversal at the frame boundary. In one implementation, this is accomplished by flipping back and forth the sign of the complex phasor used by mixer

403 to correct for Doppler shift. A set of SI and SQ results are obtained for the current subsegment while leaving the sign of the complex phasor unchanged. These results are then coherently added to corresponding entries maintained in the first set of arrays. A second set of SI and SQ results are then obtained for the current subsegment while
5 flipping the sign of the complex phasor. These results are then coherently added to corresponding entries maintained in the second set of arrays.

When this process has been completed for the current segment, peak correlator 430 is then employed to determine which of the two sets of arrays represents the greater degree of correlation with the segment. In one implementation, the array is selected which has one or more correlation values significantly higher than any of the correlation values in the other array. The hypothesis corresponding to this array is then determined to be the correct one. The sign of the complex phasor is then set accordingly, and the arrays for that hypothesis are provided to GPS processor 303 for satellite presence and range detection.

A method of operation of one embodiment of a matched filter in accordance with the subject invention is illustrated in Figures 13A-13C. Three alternative modes of operation are illustrated: alternatives A, B, and C, each involving coherent integration. Alternative A corresponds to the first mode of operation discussed above in which phase reversals at frame boundaries can be detected, and coherent integration is performed
20 across frame boundaries after account is taken of any phase reversal that may have taken place at the frame boundary.

Alternative B corresponds to the third mode of operation discussed above, in which frame boundaries, but not phase reversals, can be detected, first and second

coherent integrations are performed on either side of the frame boundary, and then the results thereof noncoherently combined.

Alternative C corresponds to the fourth mode of operation discussed above, in which frame boundaries, but not phase reversals, can be detected, coherent integration is performed across a frame boundary under two alternative hypotheses, and then the hypothesis chosen which yield the best correlation results with the segment.

The method of Figures 13A-13C will be explained in the following order:

Alternative A, Alternative B, and Alternative C.

In step 1000, a segment of samples is stored. The samples are complex samples having real and imaginary components, or equivalently, magnitude and phase components. In one implementation, each sample has I and Q components. In the matched filter of Figure 9, the segment of samples is stored in RAM 400.

In step 1001, a PN code hypothesis is selected for testing and stored in a circular shift register. In the matched filter of Figure 9, the PN code hypothesis is stored in PN code register 415.

In step 1002, a subsegment of the segment of samples stored in step 1000 is selected.

In step 1003, a Doppler shift hypothesis is selected for testing. In the matched filter of Figure 9, this step is implicitly performed by incremental Doppler generator 401 which successively generates Doppler shift hypotheses responsive to constraints or bounds imposed by a user. In one implementation example, the Doppler shift hypotheses range from $\pm 62,000$ Hz.. In another implementation example, the Doppler shift hypotheses range from $\pm 4,500$ Hz.

In step 1004, the subsegment selected in step 1002 is corrected for the Doppler shift hypothesis selected in step 1003. In the matched filter of Figure 9, this step is performed by complex mixer 403, which multiplies the subsegment of samples by a complex phasor. In one implementation example, this step is performed as described in U.S.S.N. 09/145,055, previously incorporated herein by reference.

In step 1005, the corrected data from step 1004 is stored. In the matched filter of Figure 9, the corrected data is stored in sample register 406.

In step 1006, a code phase hypothesis is selected for testing. In the matched filter of Figure 9, this step is implicit in the operation of PN code register 415 which successively and circularly shifts through each of the possible code phase hypotheses in a PN code repetition period, which, in one implementation, comprises 2046 half-chip increments.

In step 1007, the PN code hypothesis selected and stored in step 1001 is circularly shifted by an amount derived from the code phase hypothesis selected in step 1006. In the matched filter of Figure 9, the selected code phase hypothesis ranges from 0 to 2045 half-chip increments, and step 1007 is implemented by circularly shifting the PN code hypothesis by the number of half-chip increments comprising the selected code phase hypothesis.

In step 1008, the product of the shifted PN code from step 1007, and the corrected subsegment of samples from step 1004 is obtained. In one implementation, this step comprises forming the I and Q component sum of products, SI and SQ. In one implementation example, SI and SQ are derived in accordance with equations (1) and (2),

presented earlier. In the matched filter of Figure 9, this step is performed by sum of products circuitry 407.

5 In step 1009, the SI and SQ values are added to any corresponding values for the same hypotheses as applied to previous subsegments from the segment stored in step 1000. In one implementation, cumulative correlation arrays of the form shown in Figure 11 are maintained for the segment, and the SI and SQ values determined in step 1008 are added to corresponding values maintained in these arrays in accordance with the procedure illustrated in Figure 12. In the matched filter of Figure 9, this step is performed by complex adder 411, and the cumulative arrays for the segment are maintained in complex RAM 413.

10 In step 1010, a determination is made whether a frame boundary has been encountered. If so, for Alternative A, step 1014 is performed. In step 1014, a determination is made whether there is a phase reversal at the frame boundary. If so, step 1015 is performed. If not, a jump is made to step 1011. In step 1015, the sign of the complex phasor employed in step 1004 for Doppler correction is flipped. Step 1011 is then performed.

15 In step 1011, a determination is made whether there are any further code phase hypotheses which are to be tested for the selected PN code and Doppler shift hypotheses. If so, a jump is made to step 1006 and the process beginning at this point repeated for the new code phase hypothesis. If not, step 1012 is performed. In the matched filter of Figure 9, this step is implicit in the operation of PN code register 414, which successively shifts through the 2046 code phase hypotheses to be tested for a given PN code and Doppler shift hypothesis.

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5 In step 1012, a determination is made whether there are any further Doppler shift hypotheses which are to be tested for the selected PN code hypothesis. If so, a jump is made to step 1003, and the process beginning at this point repeated for the new Doppler shift hypothesis. If not, step 1013 is performed. In the matched filter of Figure 9, this step is implicit in the operation of incremental Doppler generator 401, which cycles through a plurality of Doppler shift hypotheses for a given PN code hypothesis. In one implementation example, the Doppler shift hypotheses tested for a given PN code hypothesis range from $\pm 62,000$ Hz.

66440 " 99T8220
66445 In step 1013, a determination is made whether there are any further subsegments to be analyzed for the segment which was stored in step 1000. If so, a jump is made to step 1002, and the process beginning at this point repeats itself using the new subsegment. If not, for Alternative A, the process terminates. At this point, a plurality of complex correlation values are available for further analysis, one complex value corresponding to each of the combinations of PN code, Dopple shift, and code phase hypotheses tested. In the matched filter of Figure 9, these values are stored in RAM 413, and are available to GPS processor 303 over bus 313. In one implementation example, these values are in the form of arrays as illustrated in Figure 11.

20 In one functionally-equivalent variant of the foregoing, the order of blocks 1002 and 1003 is reversed, as well as that of blocks 1012 and 1013. A benefit of this approach--processing all the subsegments first before changing the Doppler hypothesis--is that it permits a smaller RAM 400 to be used. Under the opposite ordering--in which all the Doppler hypotheses for a given subsegment are processed first--the RAM size would need to be expanded by a factor equal to the number of Doppler hypotheses.

Alternative B will now be described. Steps 1000-1009 are identical to those described earlier in relation to Alternative A, and the explanation thereof need not be repeated. In step 1010, when a frame boundary is detected, instead of branching to step 1014, for Alternative B, step 1016 is performed. In step 1016, a second set of arrays is created for the segment of interest, with entries for each of the combinations of PN code, Doppler shift, and code phase hypotheses tested. In one implementation, the second set of arrays is real rather than complex. The magnitude of each complex entry in the first set of arrays is computed by taking the square root of the sum of squares of the real and imaginary components, and the resulting value is stored in the corresponding entry in the second set of arrays. In the matched filter of Figure 9, this step is performed by circuitry 431. This procedure is repeated for each of the entries in the first set of arrays.

Step 1017 is then performed. In step 1017, each entry in the first set of arrays is zeroed out. The process then proceeds beginning with step 1011. Steps 1011-1012 are then performed in an identical manner to the like-numbered steps explained earlier in relation to Alternative A, and the explanation thereof need not be repeated here. In step 1013, if it is determined that further subsegments remain for consideration, a jump is made to step 1002, and the process repeats itself at this point. If there are no remaining subframes to be considered, steps 1018 and 1019 are performed. In step 1018, the magnitude of each of the complex values comprising the first set of arrays is computed in the manner previously described, and in step 1019, the magnitude of a value is added to the corresponding value stored in the second set of arrays. In the matched filter of Figure 9, this step is performed by circuitry 431 in combination with complex adder 411. This procedure is repeated for each of the values in the first set of arrays. At this point, the

second set of arrays comprises the correlation values for the segment. In one implementation, the second set of arrays is stored in RAM 413, and is accessible by GPS processor 303.

Alternative C will now be described. In Alternative C, steps 1000-1003 are performed in the manner described above. Step 1030 is then performed. In step 1030, a determination is made whether a complex phasor hypothesis flag has been set. As will be seen, this flag is normally cleared, and is set to a logical "1" when a frame boundary is encountered. When this event occurs, the first set of arrays being maintained for the segment is duplicated into a second set of arrays. Then, all the PN code, Doppler shift, and code phase hypotheses to be tested are run on a given subsegment twice. The first run is performed under the hypothesis or assumption that there is no phase change at the frame boundary. In the first run, the phase of the complex phasor employed in step 1004 is left unchanged. The second run is performed under the hypothesis or assumption that there is a phase change at the frame boundary. In the second run, the phase of the complex phasor employed in step 1004 is flipped.

In step 1030, if the phasor flag is not set, indicating that a frame boundary has not yet been encountered, a jump is made back to step 1004, and the process resumes as before. If the phasor flag has been set, indicating that a frame boundary has been encountered, step 1031 is performed. In step 1031, one of the two hypotheses discussed above regarding the phase change, or lack thereof, at the frame boundary is selected. Step 1032 is then performed. In step 1032, the sign of the complex phasor employed in step 1004 is either left unchanged or flipped depending on which of the two hypotheses regarding phase is selected in step 1031.

5 The process then proceeds through steps 1004-1009 in the manner described above in relation to the other alternatives. Step 1010 is then performed. In step 1010, if a frame boundary is encountered, steps 1020 and 1023 are performed. In step 1020, the complex phasor hypothesis flag discussed earlier in relation to step 1030 is set to logical “1”, and in step 1033, the data maintained in the first set of arrays being maintained for the current segment is replicated into a second set of arrays in the manner described above. The process then resumes with step 1011, which is performed as described above in relation to the other alternatives.

10 Step 1012 is then performed. In step 1012, if there are further Doppler hypotheses to be tested, the process jumps to step 1003, and the process repeats itself beginning at this point. If not, step 1034 is performed. In step 1034, a determination is made whether the complex phasor hypothesis flag is set. If so, step 1035 is performed. If not, step 1013 is performed.

15 In step 1035, a determination is made whether there are any more phase hypotheses to be tested for the current subsegment. If so, the process jumps to step 1030, and resumes at this point. If not, step 1013 is performed.

20 In step 1013, a determination is made whether there are any further subsegments to be analyzed. If so, the process jumps to step 1002, and resumes at this point. If not, step 1020 is performed. In step 1020, a determination is made which of the phase hypotheses tested is the correct one for the subsegment. In one implementation, this step is performed by selecting the hypothesis which yields correlation values that are substantially greater than correlation values for the alternate hypothesis. Once the phase hypothesis is selected, the correlation values for that hypothesis are selected as the

correlation values for the subsegment. In one implementation, in which first and second sets of arrays are maintained for two alternate phase hypotheses, the correlation data for the subsegment will comprises one or the other of the two sets of arrays.

5 Note that the foregoing description of the methods for Alternatives B and C needs to be expanded for the case in which there is more than one frame boundary in a particular segment. In that event, in the case of Alternative B, upon encountering the subsequent frame boundaries, in step 1016, the magnitude values created for the first set of arrays are added to corresponding values in the second set of arrays rather than being used to initialize those values. In the case of Alternative C, instead of just two phasor hypotheses to be tested, there will be an exponential number to be tested equal to 2^{n-1} , where n is the number of frame boundaries encountered in a segment. Accordingly, in step 1033, the first set of arrays needs to be replicated 2^{n-1} times such that each phasor hypothesis has a corresponding set of arrays maintained. In step 1020, one of the hypotheses corresponding to these arrays is then selected as the correct one.

10 A related issue is integrations performed across multiple segments. In this event, there will be a number of intervening frame boundaries (and data bits) to account for, as well as the complex phase change due to the Doppler hypothesis. As the total time span of the multiple segments increases, the spacing of the Doppler hypotheses in frequency must decrease. The net result is that each output for a given hypothesis of a given
20 segment has to be weighted by the accumulated data phase flips times the accumulated Doppler phase $e^{jw_d T}$, where T is the time of a segment relative to the first segment.

IMPLEMENTATION EXAMPLE

5 A matched filter chip code-named "Magna" which combines some of the
functionality of the sampling circuitry 308, the timing circuitry 307, and the matched
filter 310 of Figures 8 and 9 has been developed by the assignee of the subject application
(Conexant Systems, Inc. of Newport Beach, CA). A processor chip which embodies the
functionality of the GPS processor 303 of Figure 4 code-named "Scorpio", Part No.
11577-11, is available from the assignee of the subject application. In one
implementation, the processor has additional GPS-specific circuits, such as tracking
channels for continuously tracking a number of GPS satellite signals. Typically, the
processor includes at least an embedded microprocessor with an external bus. In one
configuration, the processor views the matched filter chip as a memory mapped
peripheral. It issues commands to the matched filter chip, and retrieves results after it has
completed processing for a given set of commands. An RF receiver chip which embodies
the functionality of the GPS radio receiver 300 of Figure 4 code-named "Gemini/Pices
Monopack", Part No. R6732-13, is available from the assignee of the subject
application. Additional details regarding this implementation example are available in
U.S.S.N. 09/145,055, and Lyon & Lyon Dkt. No. 241/151, previously incorporated
herein by reference.

20 In order to perform coherent integration over intervals greater than 20 ms, two
things are required. First, one needs to know where the 50 Hz data bit edges, or data
epochs (DE), occur. Second, the Doppler needs to be known to accuracy such that, over
the coherent integration period, the phase angle of the desired signal does not change
significantly.

5 The location of the data epochs can be known if the GPS time is known to an accuracy of less than 1 millisecond. This is possible because the GPS time is a time of week value and the 50 Hz data is aligned with week boundaries. If the GPS time is taken modulo 20 ms, the resulting value is the time within the current 20 ms long bit. Precise
10 GPS time can be determined from a prior solution of the GPS navigation equations, or from an outside source, such as a mobile phone system having a timing relationship to GPS time. It is also the case that each 1 ms period of the PN code, or code epoch (CE), has a precise timing relationship to the data bits. Every 20th CE is also a DE. Using this relationship, it is feasible to account for the location of the DE. This information is
15 sufficient to allow coherent integration over 20 ms intervals. If, in addition, the value of the data bit is known, the integration can be extended for longer periods, limited only by Doppler and receiver movement.

Both Doppler uncertainty and receiver motion further limit the duration over which coherent integration is effective. At a resolution of about 62 Hz, the Doppler for a
20 given operation of the matched filter cannot be more accurate than ± 31 Hz. For an error of 31 Hz, the Doppler will cause a sign reversal in the real and imaginary components of the signal after $1/31 = 32$ milliseconds. To perform Doppler hypothesis testing over longer periods than this with coherent integration requires a greater Doppler resolution than 62 Hz.

20 If it is required to coherently integrate over several 20 ms intervals, the Doppler Generator design should provide a Doppler resolution finer than 62 Hz. In general, if T is the coherent integration time in terms of actual elapsed time from the start of the first data capture to the start of the final data capture, the required Doppler resolution is $1/(2T)$.

Thus, for a one second integration time, the required Doppler resolution is 0.5 Hz or better.

In addition to Doppler, the motion of the receiver must be considered. The wavelength of the GPS signal at $L1 = 1575.42$ MHz is about 19 cm or 7.5 inches. If the receiver is in a hand held device, motion of half this distance will cause a phase inversion resulting in signal cancellation when using coherent integration. A person walking along at 4 mph will travel 3.75 inches in 53 milliseconds. Thus, a practical limit for even a slowly moving receiver may be only a few 20 ms periods. Nevertheless, if the values of the data bits are available, it is still beneficial to operate over several 20 ms periods with coherent integration in order to more rapidly improve SNR.

Figure 9 illustrates an embodiment of Magna for processing coherent integrations. A first aspect is the output of the correlation adder tree, that is, circuitry 407. Instead of processing the 1 ms coherent integrations to compute the magnitude, the complex values are directly summed into the correlation array RAM storage 413. The size of the RAM accommodates the real and imaginary values rather than only the magnitude. Since non-coherent integration may still be required in some applications, this aspect is effected with a switch. In coherent mode, the magnitude calculation is bypassed.

A second aspect is the implementation of a register 438 to hold the value of the code epoch (CE) or subsegment at which the DE occurs. This value is provided by the external processor from its knowledge of GPS time. When the DE is encountered, the Incremental Doppler generator 401 receives the flip signal 440, which causes the complex phasor to flip its sign, thus preserving the coherent integration across the data bit boundary. The flip signal is controlled by the bit value 439. If the bit value does not

cause a sign change, the flip signal-state does not change at the DE. The external processor provides the value of the bit. Note that each satellite will have a different DE and Bit register value, set by the processor before the matched filter algorithm is run for that satellite.

5 The foregoing embodiments, implementations, and implementation examples achieve a much more rapid growth in signal to noise ratio (SNR) of correlation data through the coherent integration of incremental portions or subsegments of the samples. As a result, in the case in which the invention is incorporated into a GPS receiver, the result is that desired GPS satellites are detected more quickly. Moreover, power
10 consumption is reduced due to the shorter time that the power detection circuit needs to be operational. Another result, in the case in which the GPS receiver is integrated with a mobile wireless phone, is increased call-time due to increased battery life.

 In one example, to a first order, it has been found that, by using coherent integration, a signal detector in accordance with the invention is able to achieve a 3 dB
15 improvement in SNR by increasing the processing time 200%. In contrast, a prior art signal detector employing non-coherent integration requires a 247% increase in processing time to achieve a 3 dB improvement in SNR. Moreover, this relationship is exponential. For example, to achieve a 6 dB improvement in SNR, it has been found that a signal detector in accordance with the invention requires a processing increase of 400%,
20 whereas a signal detector of the prior art requires a 610% increase in processing time.

 Another advantage of the invention is that it takes advantage of cellular and PCS phone systems and their ability to provide external sources of data useful to GPS. This data includes precise time and frequency information, and direct or indirect information

regarding data epochs (frame boundaries), and phase reversals at the frame boundaries as required for coherent integration.

Another advantage is that reliance on the matched filter of the subject invention to perform coherent integration reduces the load on the GPS processor. It also reduces the amount of RAM that the outside processor must dedicate to GPS.

Although embodiments and implementations have been described which utilize a GPS processor to perform various functions, it should be understood that embodiments are possible in which a generic processor is used to perform these functions. For purposes of this disclosure, a generic processor is defined to mean any device, including a computer, DSP, baseband processor, microprocessor, or microcomputer, which is capable of executing a discrete series of instructions stored in a memory accessible by the processor. It should also be understood that embodiments are possible in which analog circuitry is used to perform these functions.

While various embodiments of the application have been described, it will be apparent to those of ordinary skill in the art that many more embodiments and implementations are possible that are within the scope of the subject invention. Accordingly, the invention is not to be restricted except in light of the appended claims and their equivalents.

THE CLAIMS

1. A signal detector comprising:

5 a receiver for providing a segment of complex samples of a received signal comprising a desired signal perturbed by noise or pseudo-noise and subject to phase reversals at defined frame boundaries;

a multiplier configured to multiply data derived from the segment with data representative of a hypothesis regarding the signal of interest or a parameter of the signal of interest, and for providing product data representative thereof; and

10 a coherent integrator for coherently integrating the product data over a desired duration responsive to the location of a frame boundary as determined from a source other than the received signal, and deriving therefrom correlation data useful for detecting the signal of interest or a parameter thereof.

2. The signal detector of claim 1 in which the receiver is an RF receiver.

3. The signal detector is claim 1 in which the signal of interest is a carrier signal modulated with a repeating PN code.

4. The signal detector of claim 1 further comprising a hypothesis generator for generating a plurality of hypotheses.

5. The signal detector of claim 1 further comprising a processor for receiving and analyzing the correlation data.

20 6. The signal detector of claim 1 in which the source is a cellular or PCS phone network.

7. The signal detector of claim 1 further comprising a phase detector for detecting phase reversals of the signal of interest, and the coherent integrator, responsive to the

detection of a phase reversal, is configured to adjust for the phase reversal to allow coherent integration to proceed across a frame boundary.

8. The signal detector of claim 7 further comprising circuitry for, responsive to the detection of a phase reversal, flipping the sign of samples of the received signal.

5 9. The signal detector of claim 1 further comprising a frame boundary detector for detecting frame boundaries.

10. The signal detector of claim 9 wherein the coherent integrator, responsive to the detection of a frame boundary, is configured to non-coherently combine coherent integrations performed on either side of the frame boundary.

10 11. The signal detector of claim 9 wherein the coherent integrator, responsive to the detection of a frame boundary, is configured to derive first correlation data by coherently integrating the product data across the frame boundary under a first hypothesis which assumes the phase of the signal of interest is unchanged across the frame boundary, and to derive second correlation data by coherently integrating the product data across the
15 frame boundary under a second hypothesis which assumes the phase of the signal of interest flips across the frame boundary.

12. The signal detector of claim 11 further comprising circuitry selecting one of the first and second correlation based on which of the two corresponding hypotheses is more likely.

20 13. A GPS receiver including the signal detector of claim 1.

14. A method for detecting a signal comprising:

receiving a segment of complex samples of a signal comprising a signal of interest perturbed by noise or pseudo-noise and subject to phase reversals at defined frame boundaries;

5 multiplying data derived from the segment with data representative of a hypothesis regarding the signal of interest or a parameter of the signal of interest to provide product data;

detecting a frame boundary from a source other than the received signal; and
coherently integrating the product data over a desired duration responsive to the location of the frame boundary to provide correlation data useful for detecting a signal of interest or a parameter thereof.

15. The method of claim 14 wherein the signal of interest is a carrier signal modulated with a repeating PN code.

16. The method of claim 14 further comprising detecting the frame boundary from a cellular or PCS phone network.

15 17. The method of claim 14 further comprising detecting a phase reversal and adjusting the coherent integrating step responsive thereto to allow coherent integration to proceed across the frame boundary.

18. The method of claim 17 further comprising generating and testing a plurality of hypotheses.

20 19. The method of claim 14 further comprising detecting a frame boundary and, responsive thereto, non-coherently combining coherent integrations performed on either side of the frame boundary.

20. The method of claim 14 further comprising detecting a frame boundary and,
responsive thereto, deriving first correlation data by performing the coherent integration
step under a first hypothesis in which the phase of the signal of interest remains
unchanged across the frame boundary, and deriving second correlation data by
performing the coherent integration step under a second hypothesis in which the phase of
the signal of interest flips across the frame boundary.

21. The method of claim 20 further comprising selecting one of the first and second
correlation data based on a determination of which of the two corresponding hypotheses
is the correct one.

22. Computer readable media on which is stored a series of instructions embodying
the method of claim 14.

ABSTRACT OF THE DISCLOSURE

A signal detector is provided in which complex samples of a received signal are multiplied by data representative of a hypothesis, and the resulting product data is coherently integrated over a desired duration to provide correlation data representative of the level of correlation between the hypothesis and the signal. In one embodiment, the signal detector is part of a GPS receiver.

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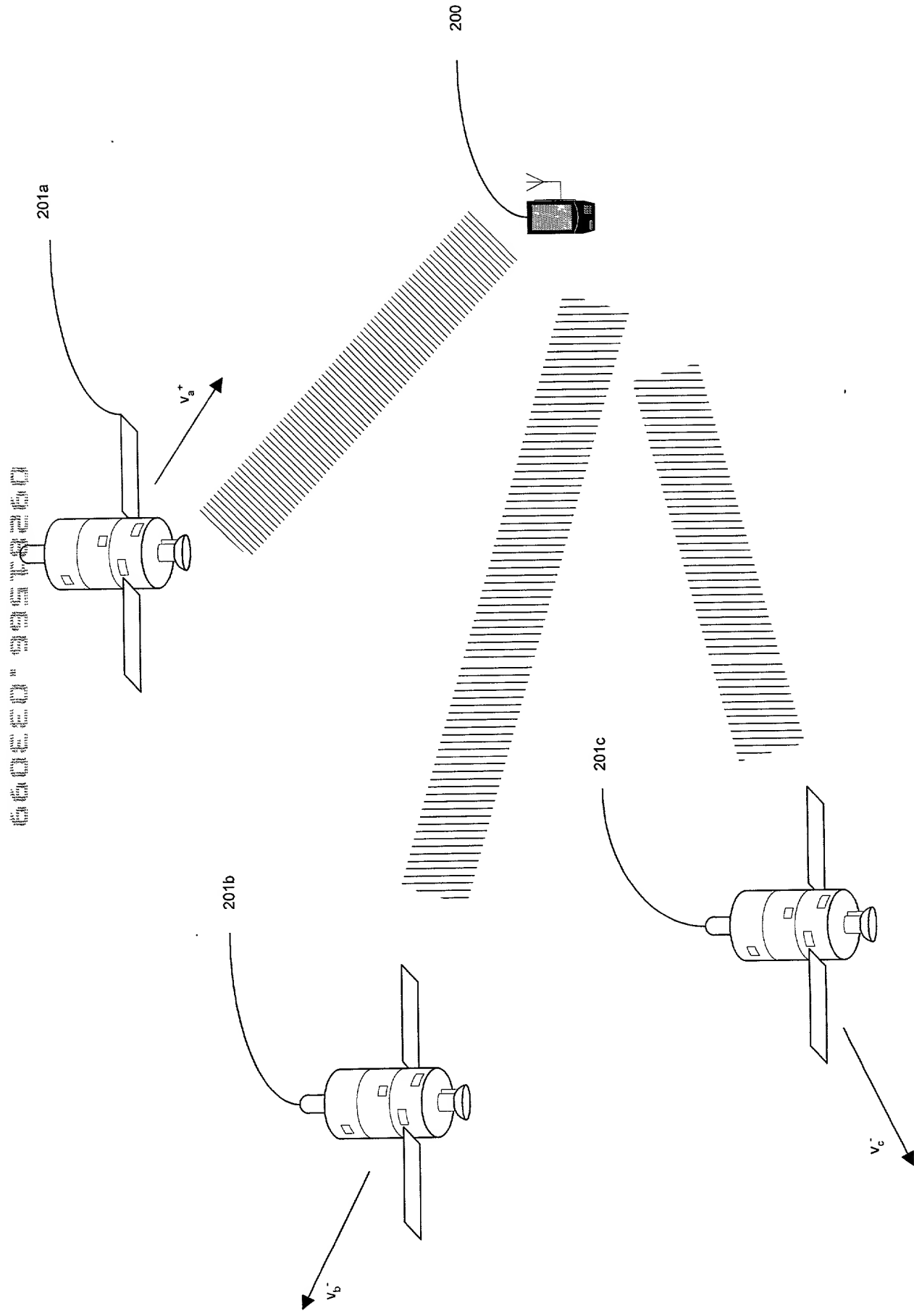


FIGURE 1

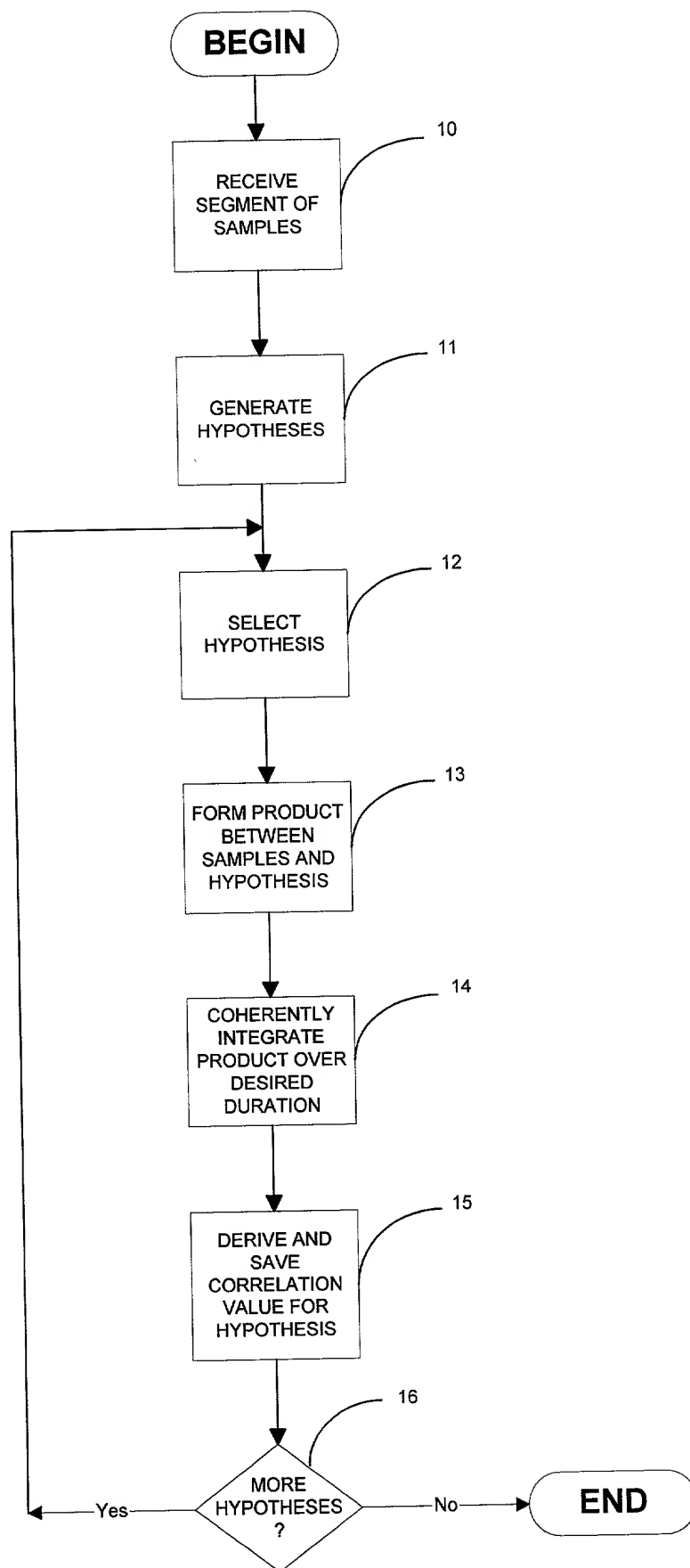


FIGURE 3

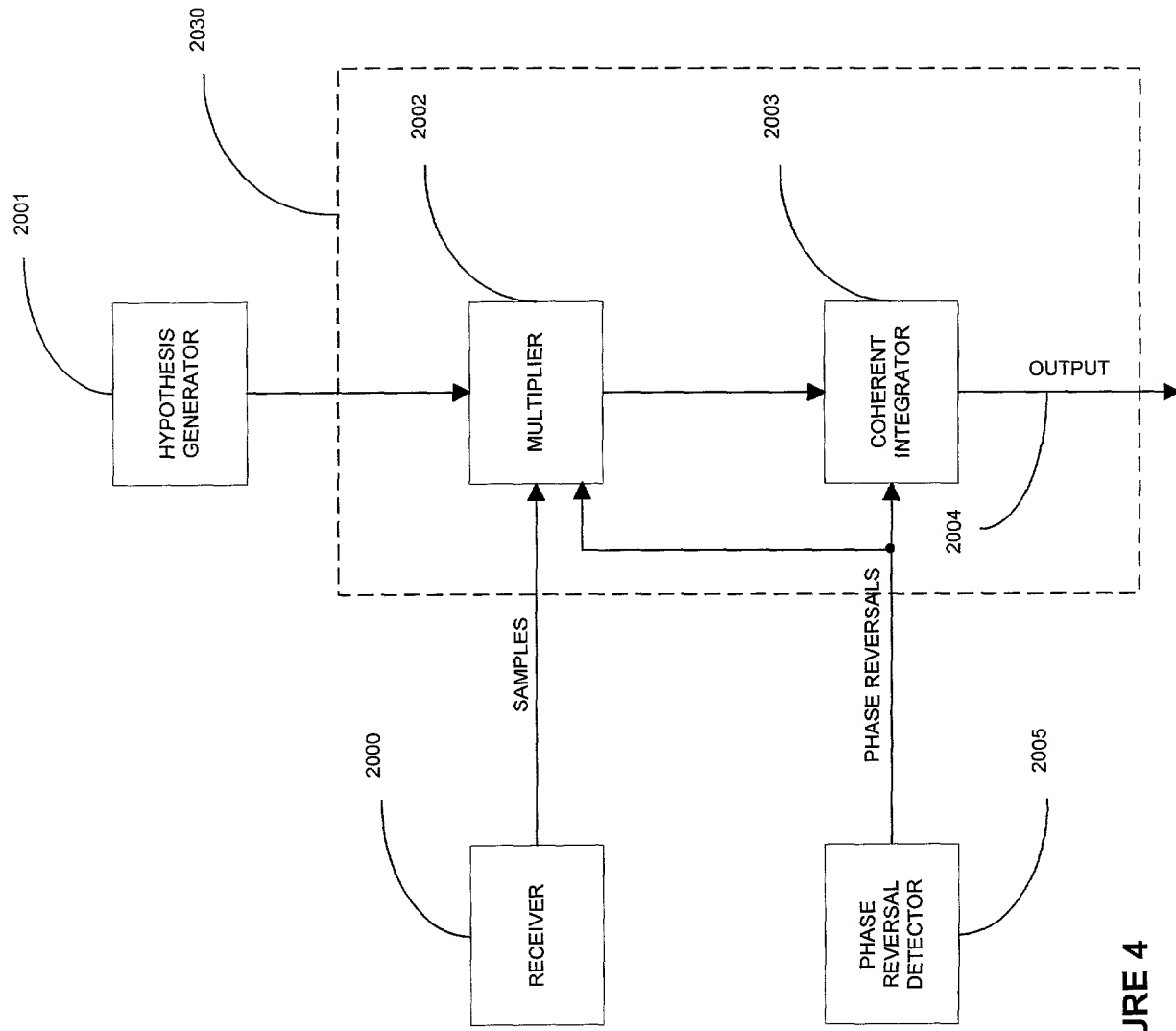


FIGURE 4

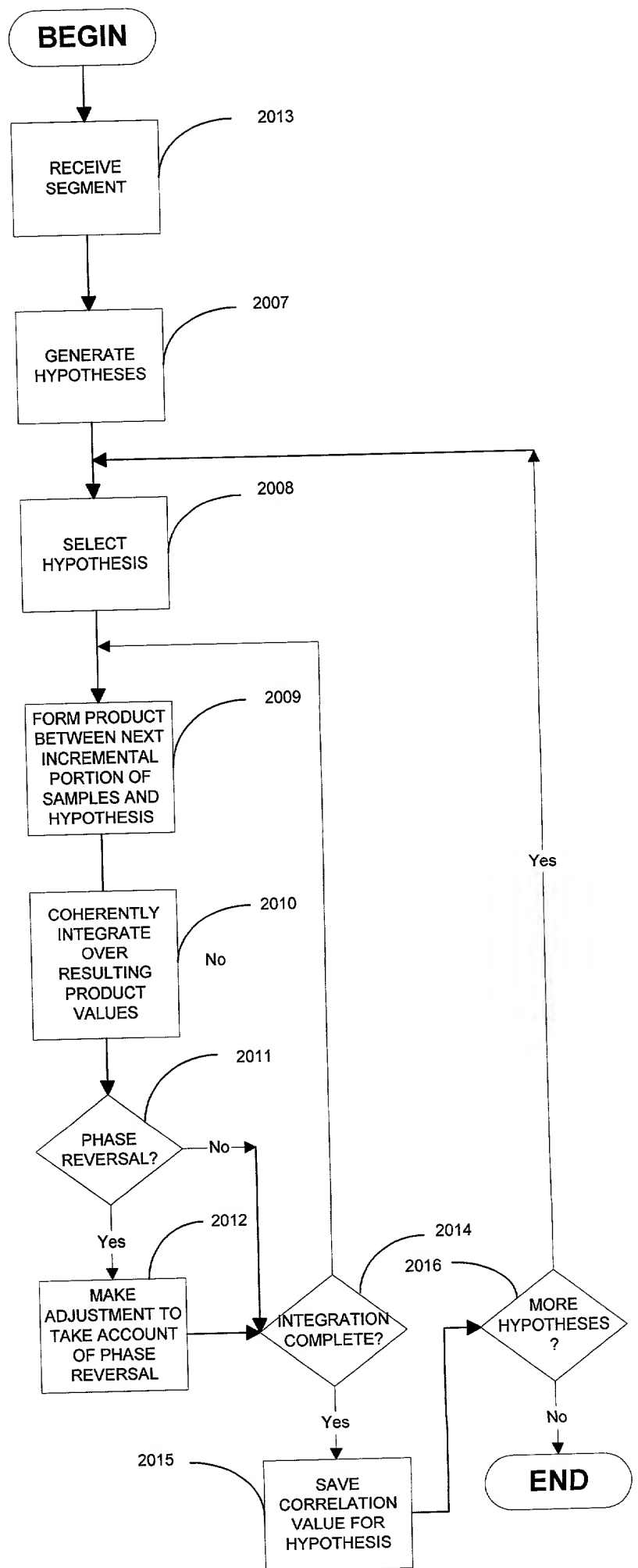


FIGURE 5

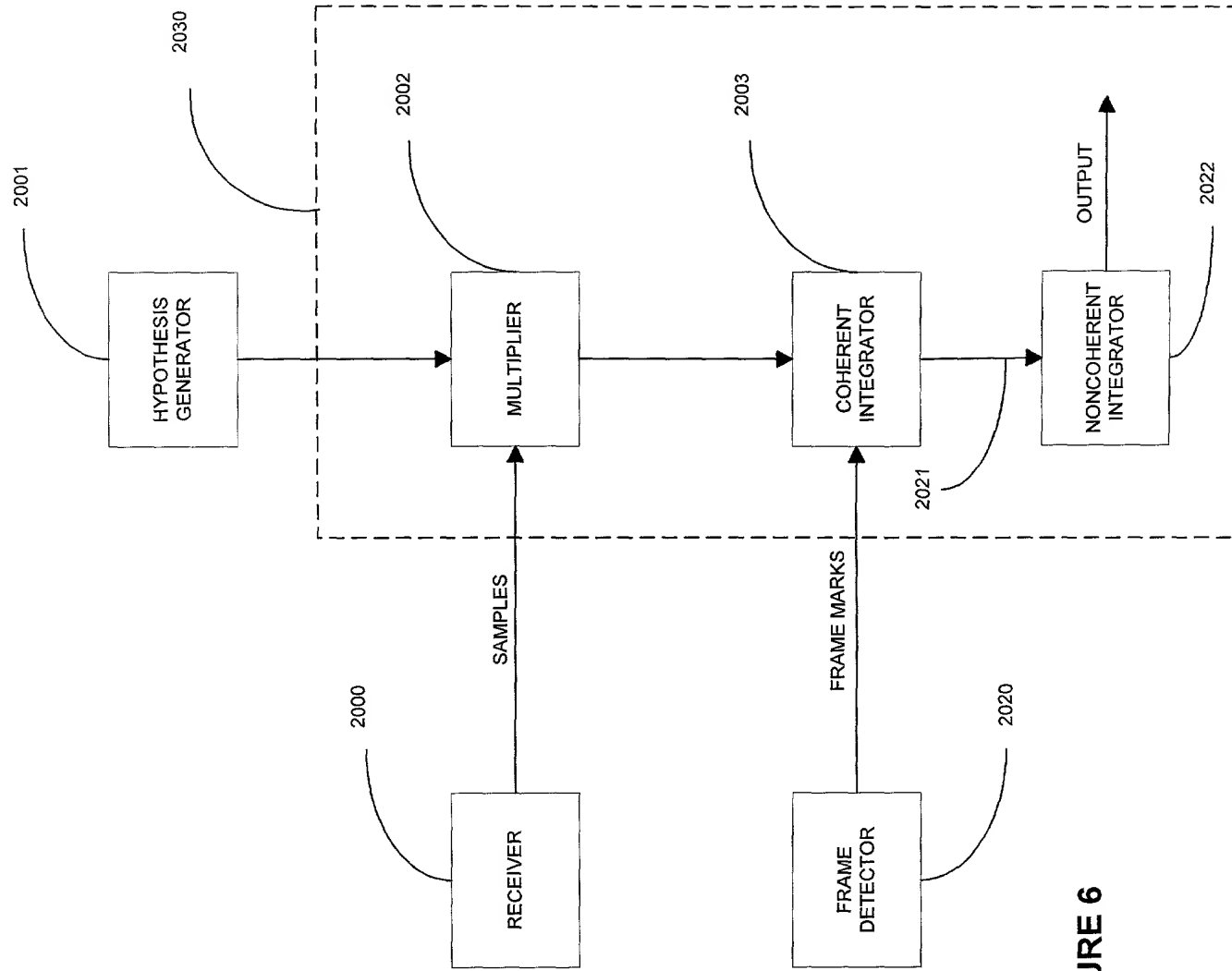


FIGURE 6

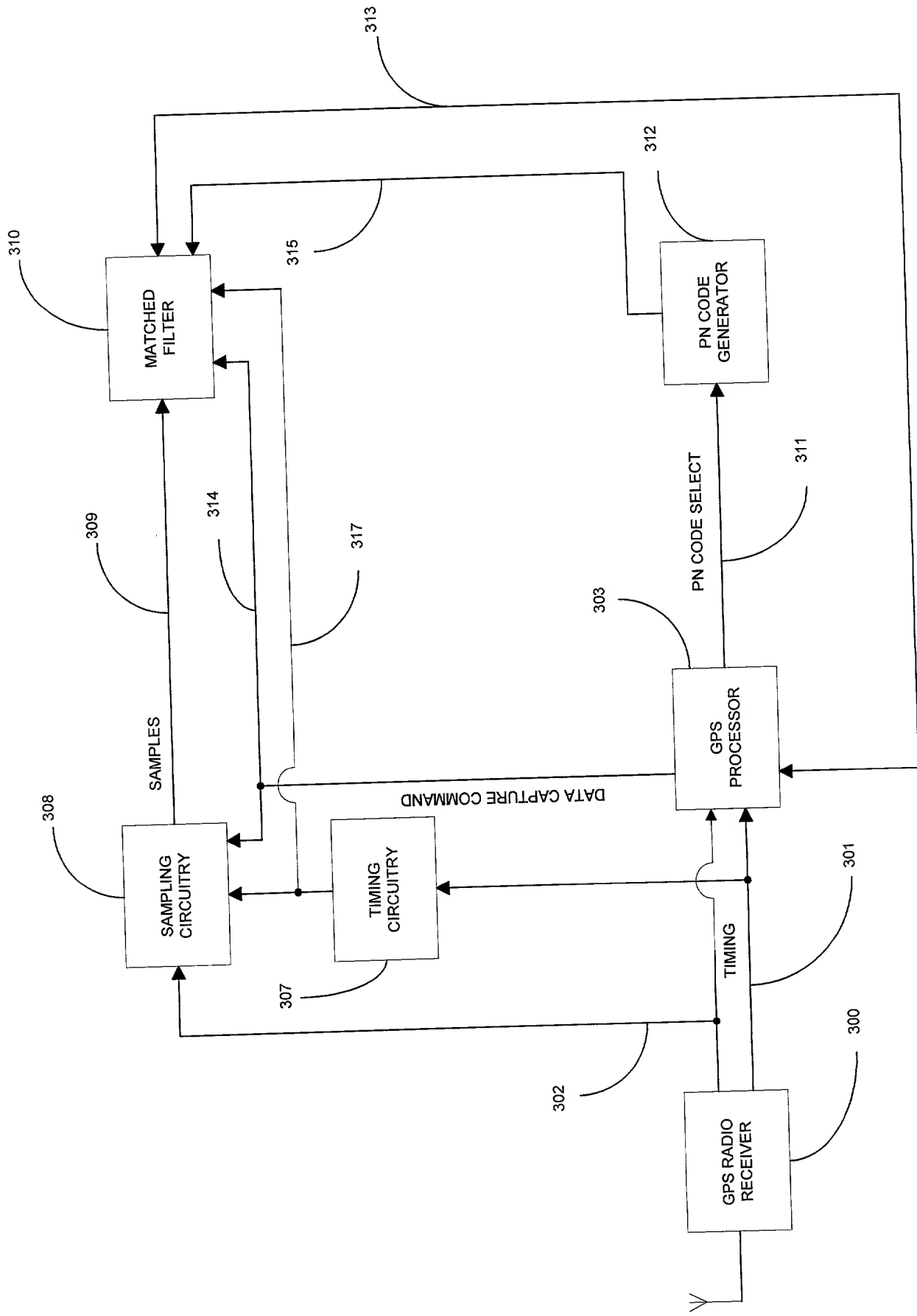
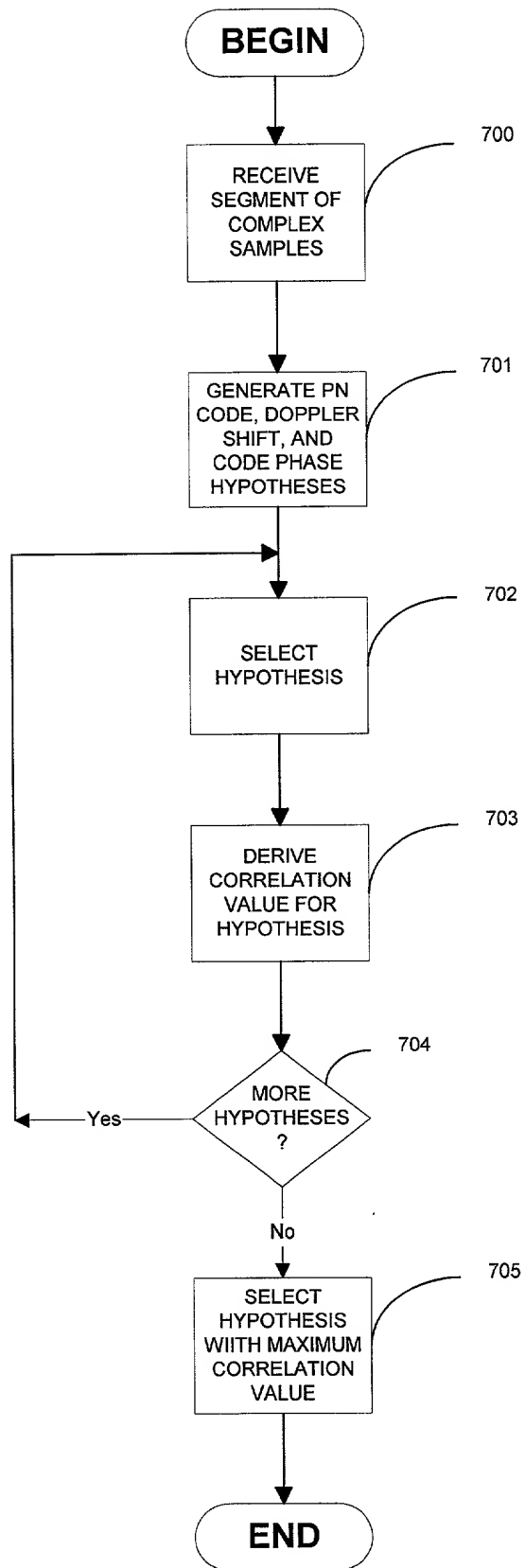


FIGURE 8

**FIGURE 10**

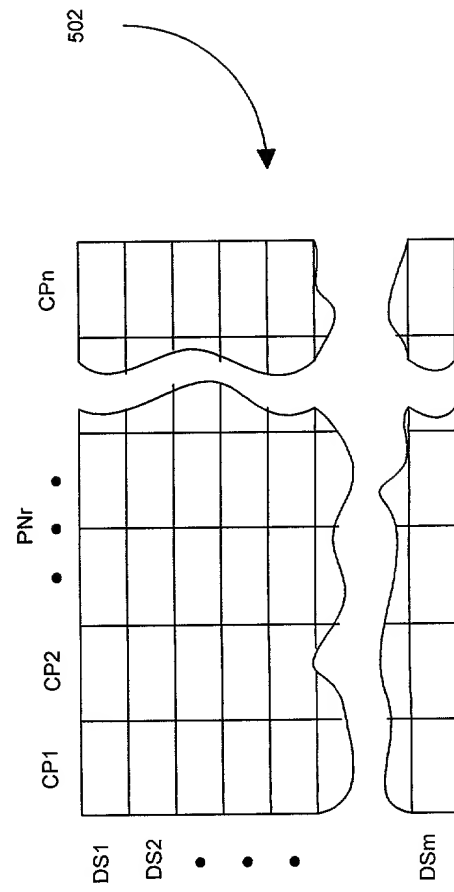
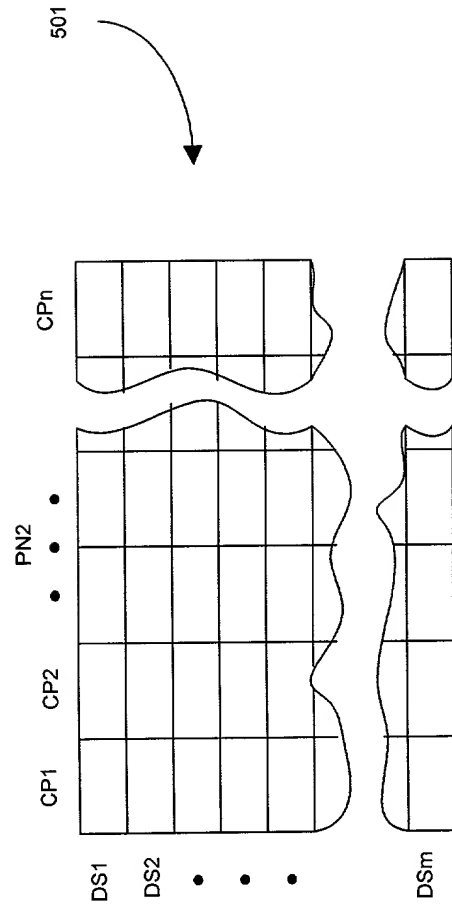
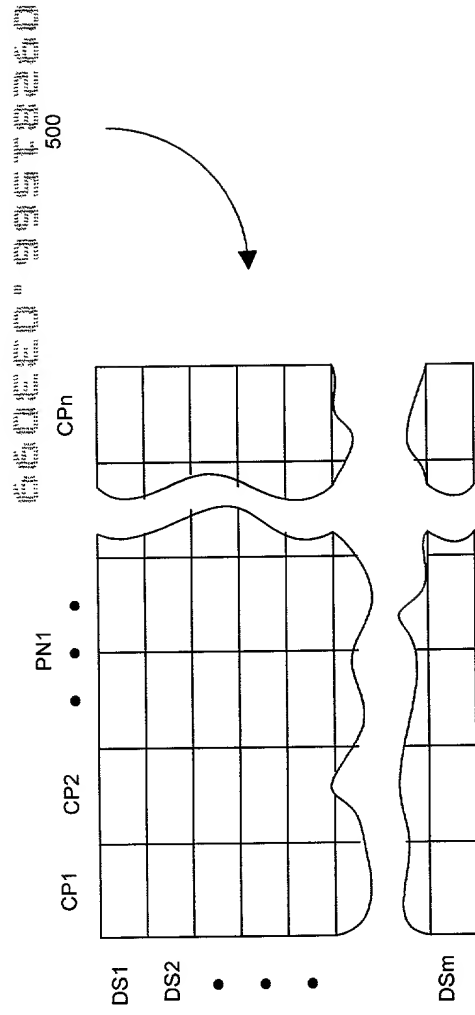


FIGURE 11

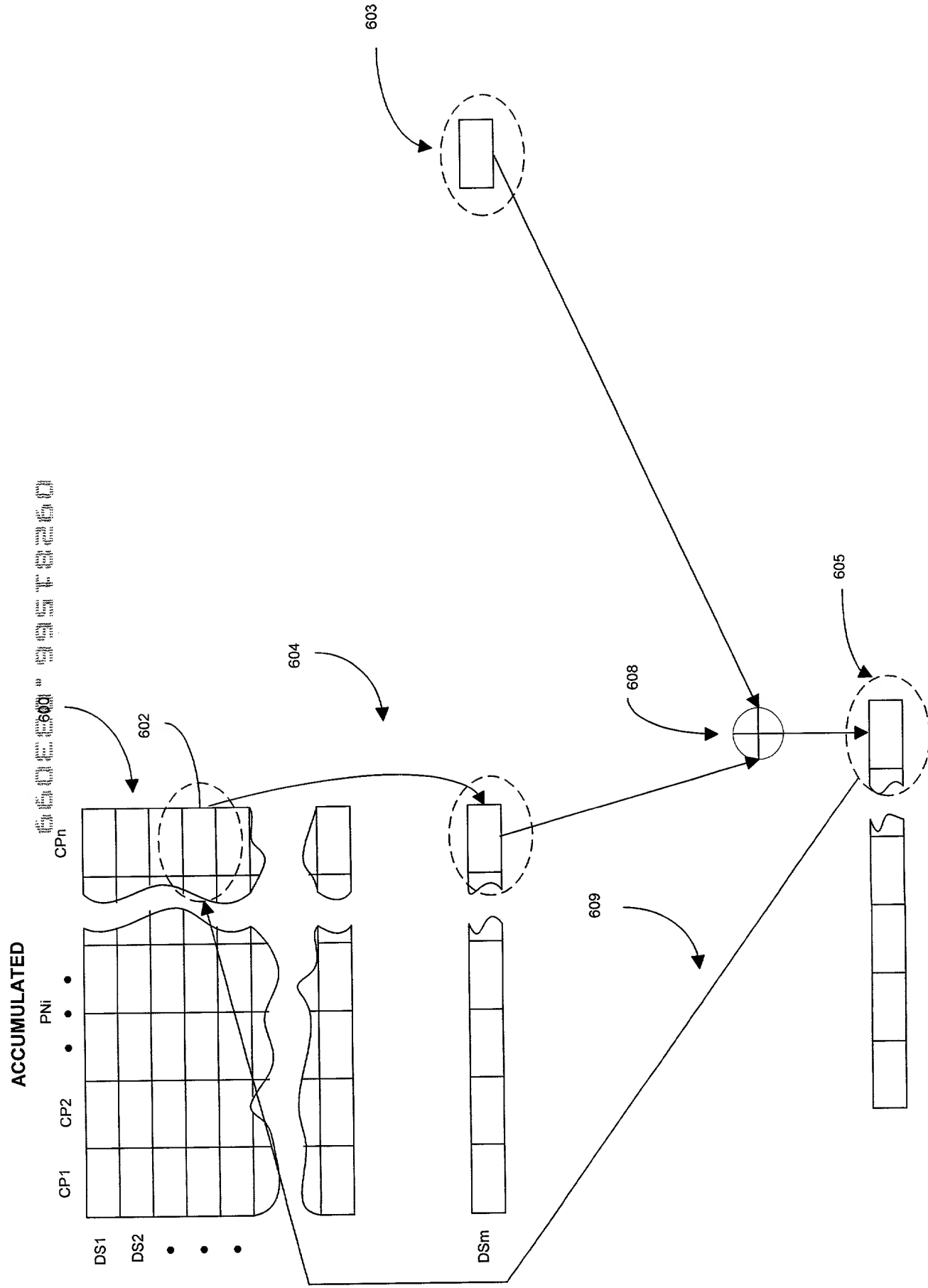
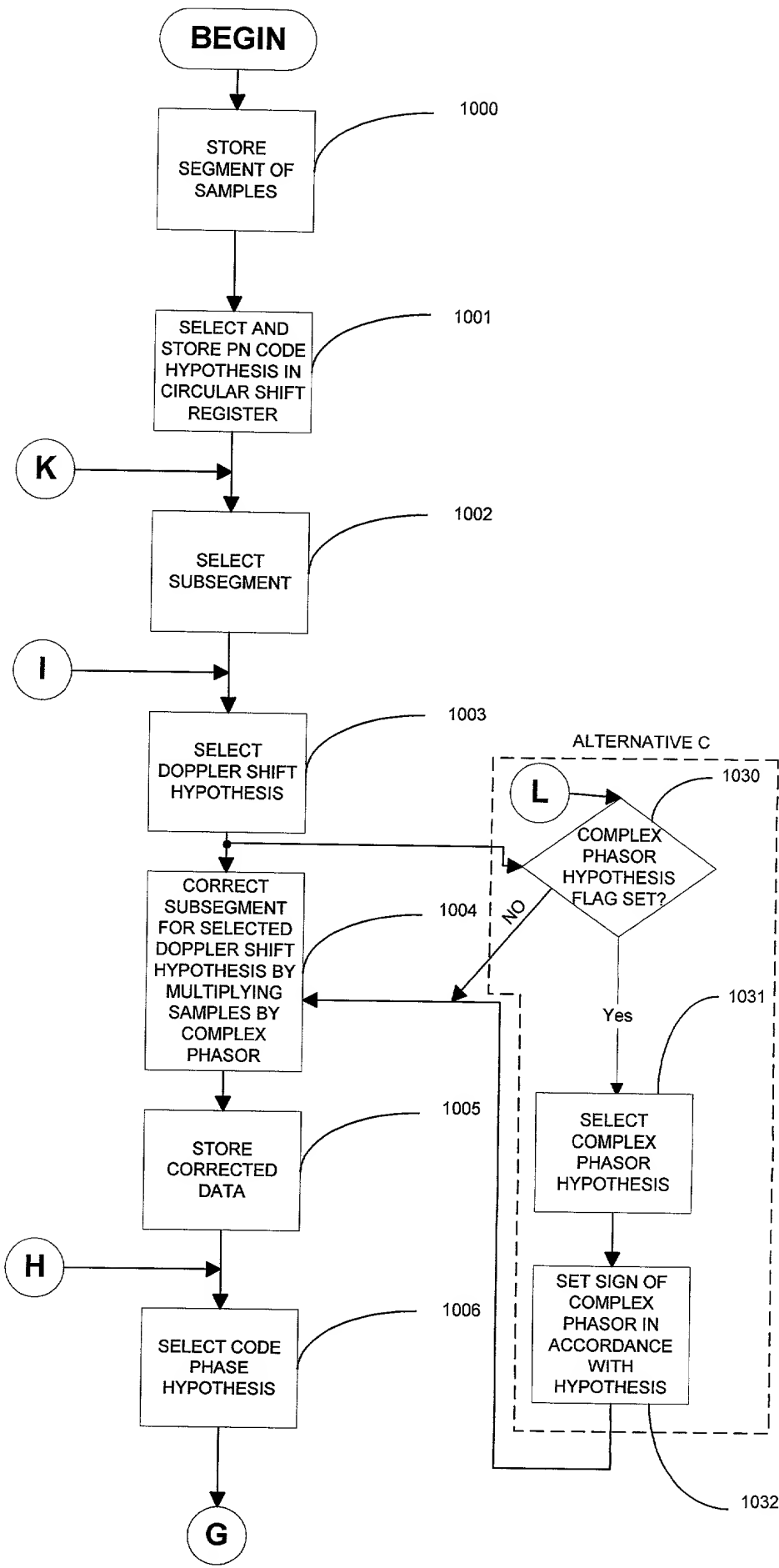


FIGURE 12

FIGURE 13A

13A
13B
13C



66000-2320

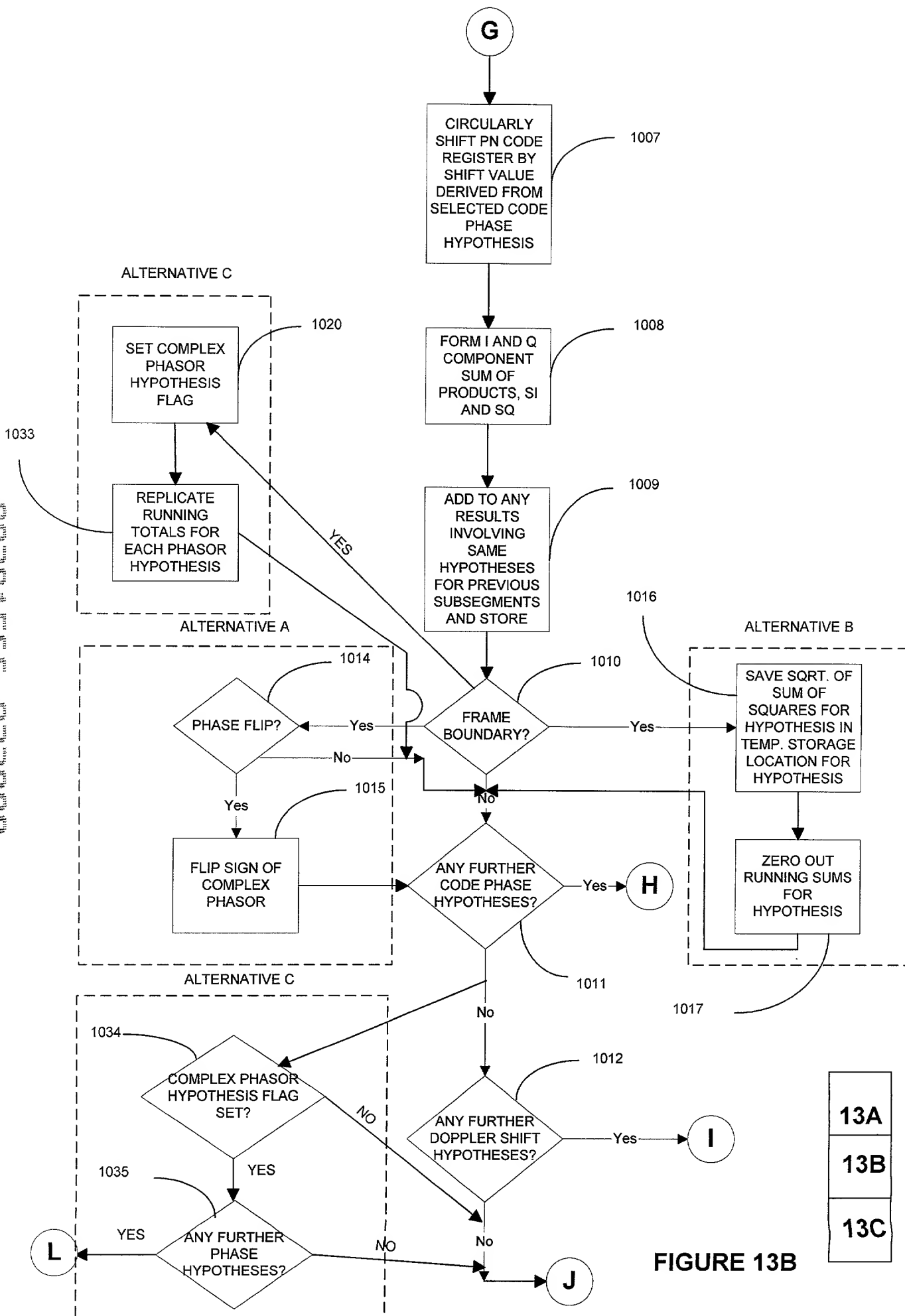
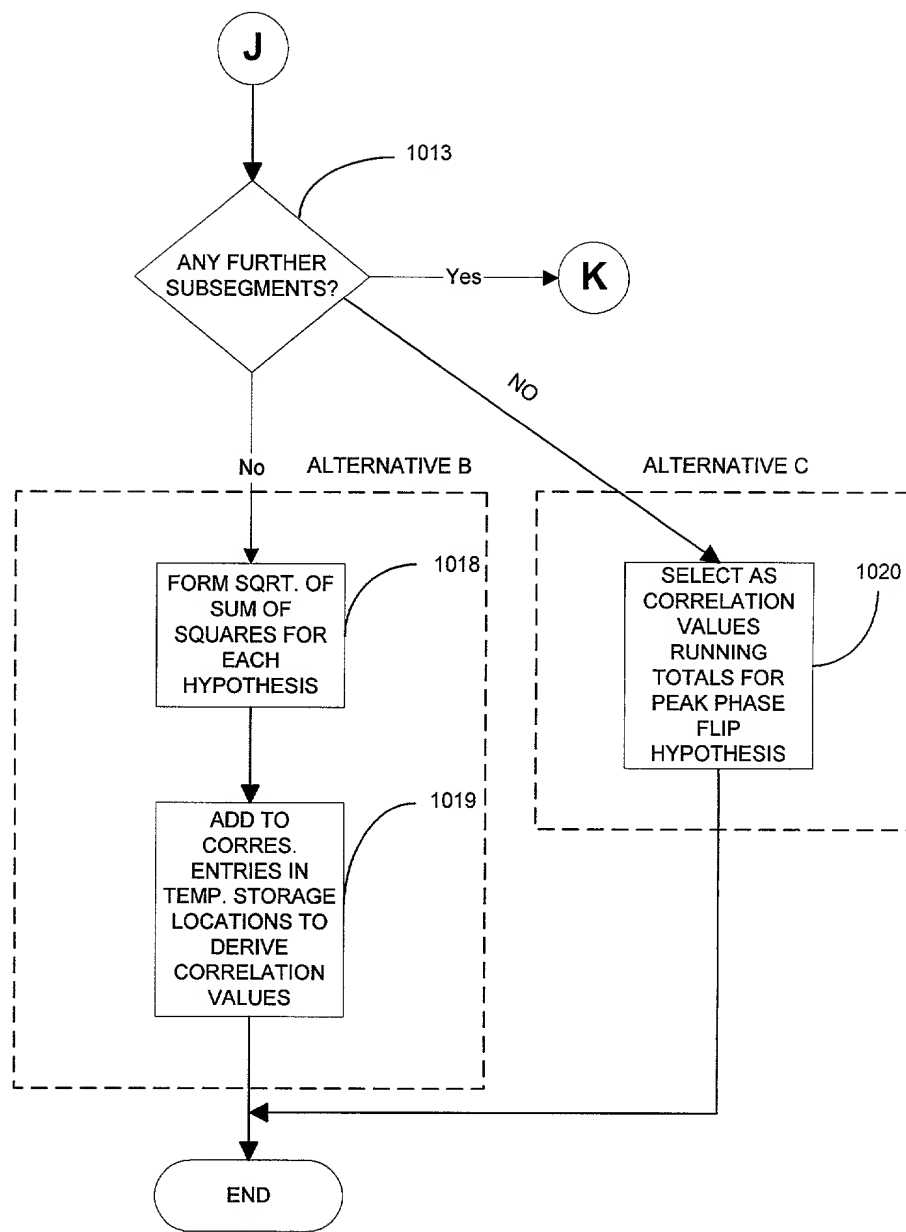


FIGURE 13B

13A

13B

13C

[illegible]

13A

13B

13C

FIGURE 13C

**DECLARATION
AND POWER OF ATTORNEY
Utility Application**

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **SIGNAL DETECTOR EMPLOYING COHERENT INTEGRATION** the specification of which

(Check One) ☒ is attached hereto OR
☐ was filed on _____ as United States Application Serial No. _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Date of Filing	Priority Claimed	
			Yes	No

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below.

Application Number(s)	Filing Date

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s), or § 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. Parent Application Number	PCT Parent Number	Parent Filing Date	Status-Patented, Pending or Abandoned

THE UNIVERSITY OF CHICAGO

Residence, post office address, citizenship and signature of inventor(s) set forth beginning on next page.

201 202 203 204 205 206

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	FULL NAME OF INVENTOR	FIRST Name	MIDDLE Initial	LAST Name	
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	POST OFFICE ADDRESS		City	State or Country	Zip Code

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Title 18, United States Code §1001, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signature of Inventor	201
Date	
Signature of Inventor	202
Date	
Signature of Inventor	203
Date	

Signature of Inventor	204
Date	
Signature of Inventor	205
Date	
Signature of Inventor	206
Date	

(Signatures should conform to names as presented at 201 et seq. above.)